FUJITSU SEMICONDUCTOR

MB91F467BA/466BA/465BA/464BA
preliminary datasheet

MB91460 series

European MCU Design Centre (EMDC)
Fujitsu Microelectronics Europe GmbH
Pittlerstr. 47
63225 Langen, Germany
Fujitsu and
Fujitsu Microelectronics Solutions Limited(FMSL)

Version 0.27**, File: mb91f467ba_shortspec_r2.0.doc**

Revision History

Version	Date	Remark
0.10	2005-09-01	Initial draft
0.11	2005-09-04	Memory map + flash memory map updated
0.12	2006-01-20	Addition of external bus interface option
0.13	2006-01-25	Corrections for external bus interface option; Remove of package information: MB91F467BA will be delivered in a QFP-144 package with pure Sn pin plating, the related package number is to be defined Use UART3 instead of UART2
0.14	2006-02-14	Upgrade tables and feature lists to refer to external bus interface option
0.15	2006-02-16	Updated pinning, added 1 USART in non-external-bus mode, exchanged WRX[1] against WRX[0]
0.16	2006-03-08	Changed pinning for 6ch CAN, 32ch ADC and NMI
0.17	2006-03-09	Corrected operation supply voltage range
0.18	2006-06-08	Delete “ESD Protection” of Electrical Characteristics Added condition of current consumption
0.19	2006-07-20	Add a postscript to “function limitation” in “2.1.Overview Table” Add the “6. IO Map”
0.20	2006-07-25	1.1.Block Diagram change IO Voltage 2.2.1.Memory Map change “not available area” 2.2.7.&2.2.8. correct memory capacity. 2.3. correct feature of “Clock supervisor” 6. Add a postscript to “function limitation” Add a Cancellation line “D/A Converter”,”Interrupt Control Unit” and “CAN 0-5 Status Flags”
	2006-08-07	4. Added “Type” in Table 6. Del a Cancellation line ”Interrupt Control Unit” Add a Cancellation line Test function (C-Unit Test, “CSVCR(bit7)”,”CANCKD”and”I-Unit Test)
	2006-08-08	6. Del a postscript(*4) It was already descripted “User’s Manual”.
0.21	2007-03-12	Added MB91F465BA information “A Cover” & 1 & 4.1 & 4.2.1 & 4.2.2 Add “MB91F465BA” 1.1 & 2.1 Add 544KB FLASH and explanation of FLASH 2.2.1 Add memory map of MB91F465BA 2.2.9 Add 544KB Fash memory map 6 Add Flash area of MB91F465BA Changed a discription about Clock supervisor 2.3 Clock supervisor function revival
0.22	2007-04-09	Added “4.3 I/O Pin Types”

0.23	2007-04-12	Added MB91F466BA/MB91F464BA information "A Cover" & 1 & 4.1 & 4.2.1 & 4.2.2 Add "MB91F466BA" and"MB91F464BA 1.1 & 2.1 Add 832KB/416KB FLASH and explanation of FLASH 2.2.1 Add memory map of MB91F466BA/MB91F464BA 2.2.9 Add 832KB/416KB Fash memory map 6 Add Flash area of MB91F466BA/MB91F464BA
	2007-04-19	Change of Chapter Constitution and Addition of "Recommended Settings" Chap1 Overview (no change) Chap2 Feature List (small change in this Chap) Chap3 Recommended Settings (addition) Chap4 IO Map (Chap6 in a previous Ver.) Chap5 Interrupt Vector Table (Chap3 in a previous Ver.) Chap6 Package and Pin Assignment (Chap4 in a previous Ver.) Chap7 Electrical Characteristics (Chap5 in a previous Ver.)
	2007-05-01	Addition of information to be related Flash (From 2.4.1 to 2.4.4)
0.24	2007-05-30	Added information of specification change about port function. 2.2.7 & 6.2.2 Add "Limitation" 2.2.7 Add "WRX1" 6.2.2 Change function of Pin44. Changed a division point of IO power supply group 6.2.1 & 6.2.2 Added package dimension in "6.1 Package"
0.25	2007-06-18	Change of initial value in "4 IO map" LVSEL (04C4h) : 00000111 -> 00000101 REGSEL(04CEh) : 00000110 -> 00000100
0.26	2007-07-24	Changed of initial value in "4 IO map" PFR00 (0D80h) : 00000000 -> 11111111 PFR01 (0D80h) : 00000000 -> 11111111 PFR02* (0D80h) : ~~00000000~~ -> ~~11111111~~ PFR03* (0D80h) : ~~00000000~~ -> ~~11111111~~ PFR04* (0D84h) : ~~00000000~~ -> ~~11111111~~ PFR05 (0D84h) : . . 000000 -> . . 111111 PFR06 (0D84h) : 00000000 -> 11111111 PFR07 (0D84h) : 00000000 -> 11111111 PFR08 (0D88h) : 0 . . 0 . . . 0 -> 1 . . 1 . . . 1 PFR09 (0D88h) : . . . . . 00 -> . . . . . 11 PFR10 (0D88h) : . . . . . 0 -> . . . . . 1 * PFR02, PFR03, and PFR04 changed only the description. Because it is a part that IO doesn't have.
0.27	2007-09-05	# 2.1 : Changed "Core" and "Resource" frequency. • Core frequency 80 MHz / 100 MHz -> 96 MHz • Resource frequency 40 MHz / 50 MHz -> 48 MHz # 2.2.2 : Changed maximum operating frequency and PLL clock multiplier method. • Core clock = "80 MHz /100 MHz" -> "96 MHz" • multiplied by 20 -> multiplied by 24

		# 3.3 ：The combination description of “CMPR : 03E9” , “Baseclk : 52MHz” and “Fmax : 96.9MHz” was deleted from the table. # 7.2 ：Parameter item in table : The maximum frequency was changed from 100MHz to 96MHz about the frequency description of “Lock-up time PLL1”.
0.27		Latest revision

Table of contents

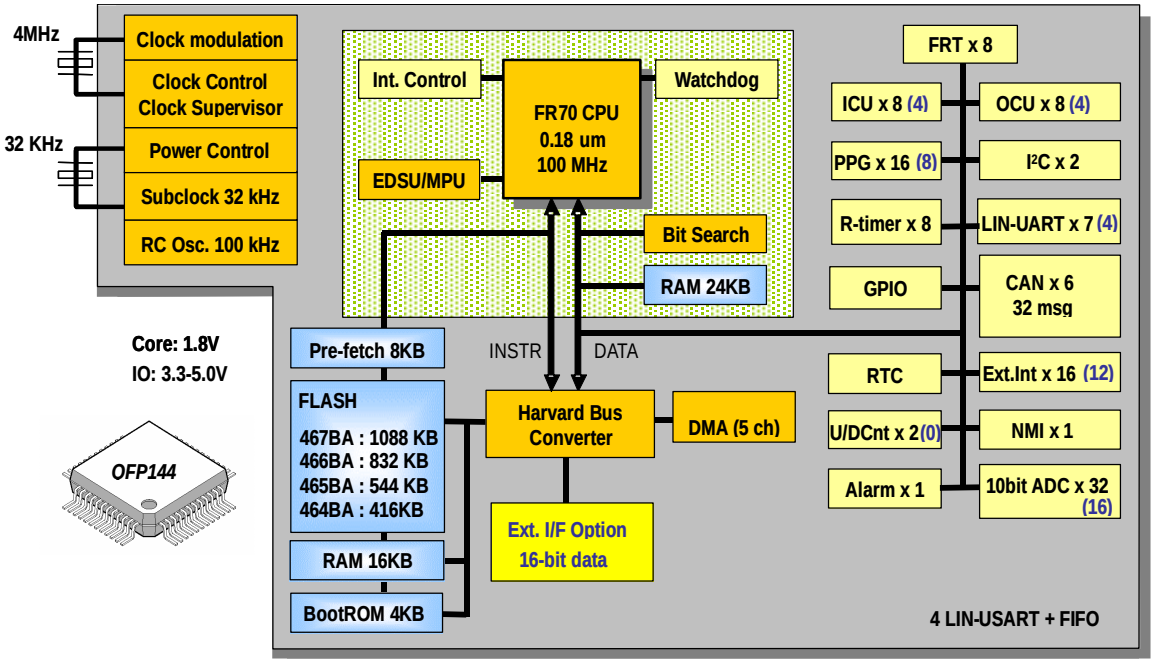
1 Overview 7
1.1 Block Diagram 7
2 Feature List 8
2.1 Overview Table 8
2.2 Core Functionality 10
2.2.1 Memory Map 11
2.2.2 FR70 CPU Core 13
2.2.3 Instruction Cache 13
2.2.4 Interrupt Controller 14
2.2.5 Internal Data RAM 14
2.2.6 Internal Program/Data RAM 14
2.2.7 External Bus Interface 14
2.2.8 DMA Controller 15
2.3 Peripheral Function 16
2.4 Embedded Program/Data Memory 21
2.4.1 Flash features 21
2.4.2 CPU Mode 22
2.4.2.1 Flash configuration in CPU mode 22
2.4.2.2 Flash access timing settings in CPU mode 24
2.4.2.3 Address mapping from CPU to parallel programming mode 25
2.4.3 Parallel flash programming mode 26
2.4.3.1 Flash configuration in parallel flash programming mode 26
2.4.3.2 Pin connections in parallel programming mode 27
2.4.4 Flash Security 28
2.4.4.1 Vector addresses 28
2.4.4.2 Security Vector FSV1 28
2.4.4.3 Security Vector FSV2 31
2.4.4.4 Register description for Flash Security 32
3 Recommended Settings 33
3.1 PLL and Clockgear settings 33
3.2 Flash interface settings 34
3.3 Clock Modulator settings 35
4 IO Map 39
5 Interrupt Vector Table 101

6 Package and Pin Assignment 109
6.1 Package 109
6.2 I/O Pins and their functions.....111
6.2.1 MB91F467BA / 466BA / 465BA / 464BA with MD_3 = 0.....111
6.2.2 MB91F467BA / 466BA / 465BA / 464BA with MD_3 = 1.....116
6.3 I/O Pin Types.....121
7 Electrical Characteristics 126
7.1 Absolute Maximum Ratings 126
7.2 Operating Conditions.....127
7.3 Converter Characteristics 129

1 Overview

The MB91F467BA/466BA/465BA/464BA are the body control flash MCU of the M91460 family. The corresponding evaluation device is the MB91V460.

1.1 Block Diagram



(x) Resources in case of bus interface option

In case of the bus interface option only the blue coloured numbers of resources will be available. The bus interface option is enabled via the pin MD_3.

2 Feature List

2.1 Overview Table

Feature	MB91V460	MB91F467BA / 466BA / 465BA / 464BA	
		MD_3 = 0	MD_3=1
Core frequency	80 MHz	96 MHz	
Resource frequency	40 MHz	48 MHz	
Watchdog	yes	yes	
Bit Search	yes	yes	
Reset Input	yes	yes	
Clock Modulator	(yes)	yes	
DMA	5 ch	5 ch	
MPU/EDSU	16 ch	8 ch	
Flash	external	1024 KB + 64 KB (MB91F467BA) 768 KB + 64 KB (MB91F466BA) 512 KB + 32 KB (MB91F465BA) 384 KB + 32 KB (MB91F464BA)	
Flash Protection	n.a.	yes	
D-bus RAM	64 KB	24 KB	
GP RAM	64 KB	16 KB	
Direct mapped cache	16 KB	8 KB	
Boot-ROM	4 kB	4 KB	
RTC	1 ch	1 ch	
Free Running Timer	8 ch	8 ch [*2]	
ICU	8 ch	8 ch	4 ch [*3]
OCU	8 ch	8 ch	4 ch [*7]
Reload Timer	8 ch	8 ch [*4]	
PPG	16 ch	16 ch	8 ch [*5]
PFM	1 ch	-	
Sound Generator	1 ch	1 ch	

Feature	MB91V460	MB91F467BA / 466BA / 465BA / 464BA	
		MD_3 = 0	MD_3=1
UpDown Counter	4 ch	2 ch	- *8
C_CAN	6 ch (128 msg buffer)	6 ch x 32 msg buffer	
LIN-USART	16 ch (4 ch FIFO)	7 ch (4 ch FIFO) *1	4 ch (4 ch FIFO)
I2C	4 ch	2 ch	
FR external bus	32-bit address / 32-bit data	-	22-bit address / 16-bit data
External Interrupts	16 ch	16 ch	12 ch *6
NMI	1 ch	1 ch	
SMC	6 ch	-	
LCD	1 ch 40x4	-	
ADC (10-bit)	32 ch	32 ch	16 ch
Alarm Comparator	2 ch	1 ch	
Low voltage detection	yes	yes	
Clock Supervisor	yes	yes	
Package	BGA 660	LQFP-144	

*1(LIN) : USART CH0(shared with external bus) can be used for asynchronous mode only.

*2(FRT) : MD3=0 → CH1&0 can't select ext. clock(bit7 of TCCS1,0)

MD3=1 → CH3,2,1&0 can't select ext. clock(bit7 of TCCS3,2,1,0)

*3 (ICU): MD3=1 → Don't set PFR = 1 & EPFR = 1 (for LIN Synch Field detect)

because there is not CH3-0 of LIN-USART.

*4 (RLT): MD3=1 → CH7,6,5&4 can't select ext. event

*5 (PPG): MD3=1 → You can use CH15-8 of PPG. CH15-12 can't select ext. trigger.

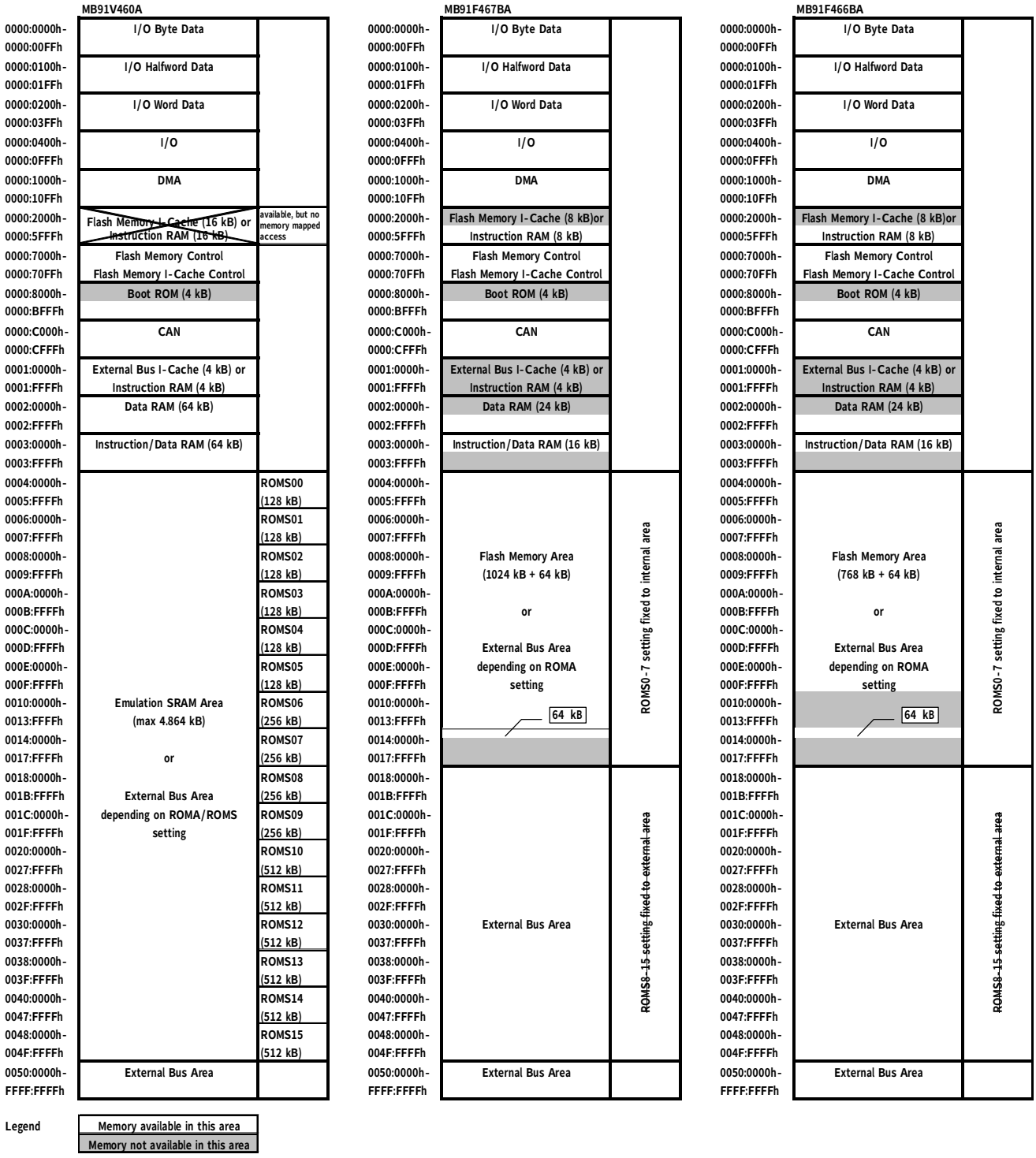
*6 (Ext-INT): INT7-4(shared with external bus) can be used for MD3=0 mode only.

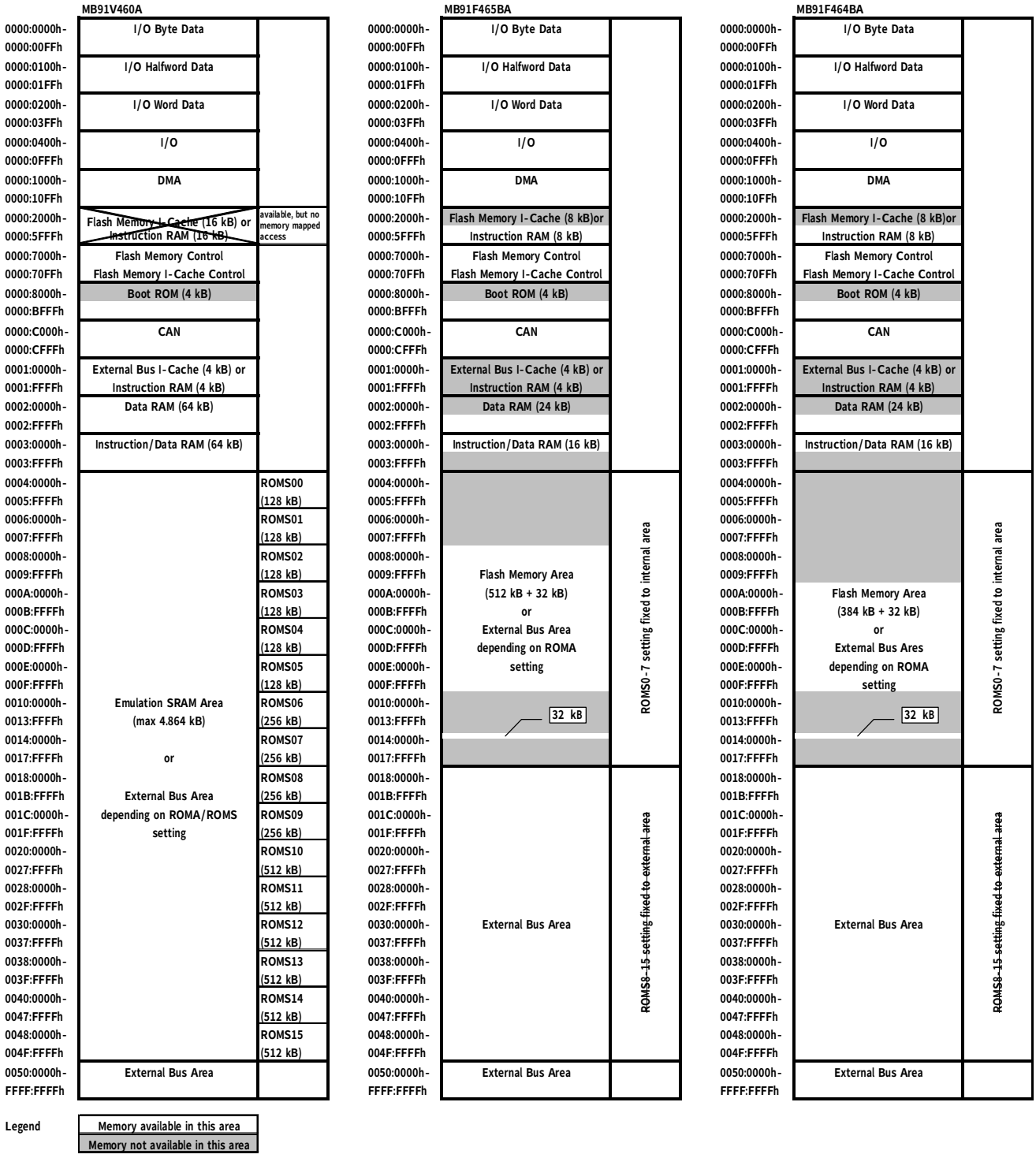
*7 (OCU): MD3=1 → You can't use ext.out-port.(but, OCU-function is active.)

*8 (UDC): MD3=1 → You can use Timer-mode only.

2.2 Core Functionality

2.2.1 Memory Map


MB91V460A
0000:0000h-0000:00FFh I/O Byte Data
0000:0100h-0000:01FFh I/O Halfword Data
0000:0200h-0000:03FFh I/O Word Data
0000:0400h-0000:0FFFh I/O
0000:1000h-0000:10FFh DMA
0000:2000h-0000:5FFFh Flash Memory I-Cache (16 kB) or Instruction RAM (16 kB)
available, but no memory mapped access
0000:7000h-0000:70FFh Flash Memory Control Flash Memory I-Cache Control
0000:8000h-0000:BFFFh Boot ROM (4 kB)
0000:C000h-0000:CFFFh CAN
0001:0000h-0001:FFFFh External Bus I-Cache (4 kB) or Instruction RAM (4 kB)
0002:0000h-0002:FFFFh Data RAM (64 kB)
0003:0000h-0003:FFFFh Instruction/Data RAM (64 kB)
0004:0000h-0005:FFFFh ROMS00 (128 kB)
0006:0000h-0007:FFFFh ROMS01 (128 kB)
0008:0000h-0009:FFFFh ROMS02 (128 kB)
000A:0000h-000B:FFFFh ROMS03 (128 kB)
000C:0000h-000D:FFFFh ROMS04 (128 kB)
000E:0000h-000F:FFFFh ROMS05 (128 kB)
0010:0000h-0013:FFFFh ROMS06 (256 kB)
0014:0000h-0017:FFFFh ROMS07 (256 kB)
0018:0000h-001B:FFFFh ROMS08 (256 kB)
001C:0000h-001F:FFFFh ROMS09 (256 kB)
0020:0000h-0027:FFFFh ROMS10 (512 kB)
0028:0000h-002F:FFFFh ROMS11 (512 kB)
0030:0000h-0037:FFFFh ROMS12 (512 kB)
0038:0000h-003F:FFFFh ROMS13 (512 kB)
0040:0000h-0047:FFFFh ROMS14 (512 kB)
0048:0000h-004F:FFFFh ROMS15 (512 kB)
Emulation SRAM Area (max 4.864 kB)
or
External Bus Area depending on ROMA/ROMS setting
0050:0000h-FFFF:FFFFh External Bus Area
MB91F467BA
0000:0000h-0000:00FFh I/O Byte Data
0000:0100h-0000:01FFh I/O Halfword Data
0000:0200h-0000:03FFh I/O Word Data
0000:0400h-0000:0FFFh I/O
0000:1000h-0000:10FFh DMA
0000:2000h-0000:5FFFh Flash Memory I-Cache (8 kB)or Instruction RAM (8 kB)
0000:7000h-0000:70FFh Flash Memory Control Flash Memory I-Cache Control
0000:8000h-0000:BFFFh Boot ROM (4 kB)
0000:C000h-0000:CFFFh CAN
0001:0000h-0001:FFFFh External Bus I-Cache (4 kB) or Instruction RAM (4 kB)
0002:0000h-0002:FFFFh Data RAM (24 kB)
0003:0000h-0003:FFFFh Instruction/Data RAM (16 kB)
0004:0000h-0007:FFFFh
0008:0000h-0009:FFFFh Flash Memory Area (1024 kB + 64 kB)
or
000A:0000h-000D:FFFFh External Bus Area depending on ROMA setting
000E:0000h-0013:FFFFh 64 kB
0014:0000h-0017:FFFFh
ROMS0-7 setting fixed to internal area
0018:0000h-001B:FFFFh
001C:0000h-001F:FFFFh
0020:0000h-0027:FFFFh
0028:0000h-002F:FFFFh
0030:0000h-0037:FFFFh External Bus Area
0038:0000h-003F:FFFFh
0040:0000h-0047:FFFFh
0048:0000h-004F:FFFFh
ROMS8-15 setting fixed to external area
0050:0000h-FFFF:FFFFh External Bus Area
MB91F466BA
0000:0000h-0000:00FFh I/O Byte Data
0000:0100h-0000:01FFh I/O Halfword Data
0000:0200h-0000:03FFh I/O Word Data
0000:0400h-0000:0FFFh I/O
0000:1000h-0000:10FFh DMA
0000:2000h-0000:5FFFh Flash Memory I-Cache (8 kB)or Instruction RAM (8 kB)
0000:7000h-0000:70FFh Flash Memory Control Flash Memory I-Cache Control
0000:8000h-0000:BFFFh Boot ROM (4 kB)
0000:C000h-0000:CFFFh CAN
0001:0000h-0001:FFFFh External Bus I-Cache (4 kB) or Instruction RAM (4 kB)
0002:0000h-0002:FFFFh Data RAM (24 kB)
0003:0000h-0003:FFFFh Instruction/Data RAM (16 kB)
0004:0000h-0007:FFFFh
0008:0000h-0009:FFFFh Flash Memory Area (768 kB + 64 kB)
or
000A:0000h-000D:FFFFh External Bus Area depending on ROMA setting
000E:0000h-0013:FFFFh 64 kB
0014:0000h-0017:FFFFh
ROMS0-7 setting fixed to internal area
0018:0000h-001B:FFFFh
001C:0000h-001F:FFFFh
0020:0000h-0027:FFFFh
0028:0000h-002F:FFFFh
0030:0000h-0037:FFFFh External Bus Area
0038:0000h-003F:FFFFh
0040:0000h-0047:FFFFh
0048:0000h-004F:FFFFh
ROMS8-15 setting fixed to external area
0050:0000h-FFFF:FFFFh External Bus Area
Legend
Memory available in this area
Memory not available in this area


MB91V460A
0000:0000h-0000:00FFh I/O Byte Data
0000:0100h-0000:01FFh I/O Halfword Data
0000:0200h-0000:03FFh I/O Word Data
0000:0400h-0000:0FFFh I/O
0000:1000h-0000:10FFh DMA
0000:2000h-0000:5FFFh Flash Memory I-Cache (16 kB) or Instruction RAM (16 kB)
available, but no memory mapped access
0000:7000h-0000:70FFh Flash Memory Control Flash Memory I-Cache Control
0000:8000h-0000:BFFFh Boot ROM (4 kB)
0000:C000h-0000:CFFFh CAN
0001:0000h-0001:FFFFh External Bus I-Cache (4 kB) or Instruction RAM (4 kB)
0002:0000h-0002:FFFFh Data RAM (64 kB)
0003:0000h-0003:FFFFh Instruction/Data RAM (64 kB)
0004:0000h-0005:FFFFh ROMS00 (128 kB)
0006:0000h-0007:FFFFh ROMS01 (128 kB)
0008:0000h-0009:FFFFh ROMS02 (128 kB)
000A:0000h-000B:FFFFh ROMS03 (128 kB)
000C:0000h-000D:FFFFh ROMS04 (128 kB)
000E:0000h-000F:FFFFh ROMS05 (128 kB)
0010:0000h-0013:FFFFh ROMS06 (256 kB)
0014:0000h-0017:FFFFh ROMS07 (256 kB)
0018:0000h-001B:FFFFh ROMS08 (256 kB)
001C:0000h-001F:FFFFh ROMS09 (256 kB)
0020:0000h-0027:FFFFh ROMS10 (512 kB)
0028:0000h-002F:FFFFh ROMS11 (512 kB)
0030:0000h-0037:FFFFh ROMS12 (512 kB)
0038:0000h-003F:FFFFh ROMS13 (512 kB)
0040:0000h-0047:FFFFh ROMS14 (512 kB)
0048:0000h-004F:FFFFh ROMS15 (512 kB)
Emulation SRAM Area (max 4.864 kB)
or
External Bus Area depending on ROMA/ROMS setting
0050:0000h-FFFF:FFFFh External Bus Area
MB91F465BA
0000:0000h-0000:00FFh I/O Byte Data
0000:0100h-0000:01FFh I/O Halfword Data
0000:0200h-0000:03FFh I/O Word Data
0000:0400h-0000:0FFFh I/O
0000:1000h-0000:10FFh DMA
0000:2000h-0000:5FFFh Flash Memory I-Cache (8 kB)or Instruction RAM (8 kB)
0000:7000h-0000:70FFh Flash Memory Control Flash Memory I-Cache Control
0000:8000h-0000:BFFFh Boot ROM (4 kB)
0000:C000h-0000:CFFFh CAN
0001:0000h-0001:FFFFh External Bus I-Cache (4 kB) or Instruction RAM (4 kB)
0002:0000h-0002:FFFFh Data RAM (24 kB)
0003:0000h-0003:FFFFh Instruction/Data RAM (16 kB)
0004:0000h-0009:FFFFh
Flash Memory Area (512 kB + 32 kB) or External Bus Area depending on ROMA setting
32 kB
ROMS0-7 setting fixed to internal area
0014:0000h-0017:FFFFh
0018:0000h-001B:FFFFh
001C:0000h-001F:FFFFh
0020:0000h-0027:FFFFh
0028:0000h-002F:FFFFh
0030:0000h-0037:FFFFh
0038:0000h-003F:FFFFh
0040:0000h-0047:FFFFh
0048:0000h-004F:FFFFh
External Bus Area
ROMS8-15 setting fixed to external area
0050:0000h-FFFF:FFFFh External Bus Area
MB91F464BA
0000:0000h-0000:00FFh I/O Byte Data
0000:0100h-0000:01FFh I/O Halfword Data
0000:0200h-0000:03FFh I/O Word Data
0000:0400h-0000:0FFFh I/O
0000:1000h-0000:10FFh DMA
0000:2000h-0000:5FFFh Flash Memory I-Cache (8 kB)or Instruction RAM (8 kB)
0000:7000h-0000:70FFh Flash Memory Control Flash Memory I-Cache Control
0000:8000h-0000:BFFFh Boot ROM (4 kB)
0000:C000h-0000:CFFFh CAN
0001:0000h-0001:FFFFh External Bus I-Cache (4 kB) or Instruction RAM (4 kB)
0002:0000h-0002:FFFFh Data RAM (24 kB)
0003:0000h-0003:FFFFh Instruction/Data RAM (16 kB)
0004:0000h-0009:FFFFh
Flash Memory Area (384 kB + 32 kB) or External Bus Ares depending on ROMA setting
32 kB
ROMS0-7 setting fixed to internal area
0014:0000h-0017:FFFFh
0018:0000h-001B:FFFFh
001C:0000h-001F:FFFFh
0020:0000h-0027:FFFFh
0028:0000h-002F:FFFFh
0030:0000h-0037:FFFFh
0038:0000h-003F:FFFFh
0040:0000h-0047:FFFFh
0048:0000h-004F:FFFFh
External Bus Area
ROMS8-15 setting fixed to external area
0050:0000h-FFFF:FFFFh External Bus Area
Legend
Memory available in this area
Memory not available in this area

2.2.2 FR70 CPU Core

- 32-bit RISC, load/store architecture, pipeline 5 stages
- Maximum operating frequency: Core clock = 96 MHz (device dependent)
  (Source oscillation= 4 MHz, multiplied by 24 (PLL clock multiplier method))
- General-purpose registers: 16 x 32 bits
- 16-bit fixed-length instruction (Base instruction)
- 32-bit linear address space: 4 Gbytes
- Instructions suitable for embedded application
  - Transfer command between memories
  - Bit-processing instruction
  - Barrel-shift instructions
- Instructions supporting C-language
- Function's enter command /exit command
- Multi-load/store command of register contents
- Assembler statement is also easily available
  Register's interlock function
- Multiplier's embedded application/command level support
  - Signed 32-bit multiplication: 5 cycles
  - Signed 16-bit multiplication: 3 cycles
- Interrupt (PC/PS are saved): 6 cycles (16 priority level)
- Harvard architecture enables simultaneous execution of program access and data access
- Memory protection function
- Embedded debug support
- Commands compatible with FR family

2.2.3 Instruction Cache

- Direct mapped I-cache
  - 8 KByte integrated
  - Lock function enabling programs to be resident

2.2.4 Interrupt Controller

- A total of 16 external interrupt lines (8 normal interrupt pins, 8 interrupt pins shared with peripheral inputs for Wake Up from STOP mode, i.e. CAN RX and I^2C SDA)
- Interrupts from internal peripherals (128 interrupt vectors)
- Priority levels programmable for normal interrupt lines excluding the non-maskable one (16 levels)
- Capable of using the normal interrupt pins for Wake Up from STOP mode

2.2.5 Internal Data RAM

- 24 KBytes integrated
- Zero wait state for read/write access

2.2.6 Internal Program/Data RAM

- 16 kBytes integrated
- Zero wait state for read/write access of instructions
- One wait state for read/write access of data

2.2.7 External Bus Interface

- If the mode pin MD_3 is set to “1”an external bus interface will become available instead of several resources.
- The external bus interface will include 16 data lines, 22 address lines, two chip select lines, CLK, RDY, RDX, WRX0 and WRX1.

********** Limitation **********

In MB91F467BA/466BA/465BA/464BA, you can not use Pin44 as general purpose port

in a state of “MD_3 = 1”. It means that Pin44 is able to use only as “WRX1”.

(For a description of I/O Ports please refer to Hardware Manual chapter 55.)

****

2.2.8 DMA Controller

- Four transfer modes supported: single/block, burst, continuous transfer, and fly-by
- 5 channels
- 3 types of transfer sources (external pins/internal peripherals/and software)
- Up to 128 selectable internal transfer sources
- Addressing mode: Specifying up to 32-bit addresses (Increment/decrement/fixed)
- Transfer mode (Demand transfer/burst transfer/step transfer/block transfer)
- Transferred data size selectable from among 8, 16, and 32 bits

2.3 Peripheral Function

- General-purpose port: All functional pins can be used as general-purpose ports, if the corresponding function is not needed.
  - N channel open drain port out of above: 4 (for I^2C)

- A/D converter : 32 channels (1 unit) / 16 channels in case of MD_3 = 1
  - Series-parallel type
  - Resolution: 10 bits
  - Minimum conversion time: 3μs
  - Single conversion mode
  - Continuous conversion mode
  - Stop conversion mode
  - Activation by software or external trigger can be selected
  - Reload timer 7 and A/D Converter co-operate

- Alarm comparator : 1 channel
  - Monitors an external voltage and generates an interrupt in case of a voltage lower or higher than the defined thresholds
  - Status is readable, interrupts can be masked separately

- External interrupt input : 16 channels / 12 channels in case of MD_3 = 1
  - Can be programmed to be edge sensitive or level sensitive
  - Interrupt mask and request pending bits per channel
  - 4 channels combined with CAN RX for wakeup
  - 2 channels combined with I^2C SDA for wakeup

- Non maskable interrupt (NMI) : 1 channel
  - Highest priority of all user interrupts

- Bit search module (using REALOS)
  - Function to search the first bit position of “1”, “0”, “Changed” from MSB (most significant bit) within 1 word

- Up/down counter : 16 bits x 2 channels / Not available in case of MD_3 = 1
  - Timer mode, up/down count mode, phase difference mode (x2, x4)
  - Includes clock prescaler ($f_{RES}/2^1$, $f_{RES}/2^3$)

- Reload timer : 16 bits x 8 channels
  - 16-bit reload counter
  - Includes clock prescaler ($f_{RES}/2^1$, $f_{RES}/2^3$, $f_{RES}/2^5$, $f_{RES}/2^6$, $f_{RES}/2^7$)

- Free-run timer : 16 bits x 8 channels
  - 16-bit free running counter, signals an interrupt when overflow or match with compare register
  - Includes prescaler ($f_{RES}/2^2$, $f_{RES}/2^4$, $f_{RES}/2^5$, $f_{RES}/2^6$)
  - Timer data register has R/W access

- PPG : 16 bit x 16 channels / 16-bit x 8 channels in case of MD_3 = 1
  - 16 bit down counter, cycle and duty setting registers
  - Interrupt at triggering, cycle or duty match
  - PWM operation and one-shot operation
  - Internal prescaler allows $f_{RES}/2^0$, $f_{RES}/2^2$, $f_{RES}/2^4$, $f_{RES}/2^6$ as counter clock
  - Can be triggered by software, reload timer or external trigger event
  - Reload timer 0/1 available as trigger for PPG 0/1/2/3
  - Reload timer 2/3 available as trigger for PPG 4/5/6/7
  - Reload timer 4/5 available as trigger for PPG 8/9/10/11
  - Reload timer 6/7 available as trigger for PPG 12/13/14/15

- Input capture : 16 bits x 8 channels / 4 channels in case of MD_3 = 1
  - Rising edge, falling edge or rising & falling edge sensitive
  - Free-run timer 0 and input capture 0/1 co-operate
  - Free-run timer 1 and input capture 2/3 co-operate
  - Free-run timer 4 and input capture 4/5 co-operate
  - Free-run timer 5 and input capture 6/7 co-operate

- Output compare : 16 bits x 8 channels / 4 channels in case of MD_3 = 1
  - Signals an interrupt when a match with of 16-bit IO timer occurs
  - An output signal can be generated
  - Free-run timer 2 and output compare 0/1 co-operate
  - Free-run timer 3 and output compare 2/3 co-operate
  - Free-run timer 6 and output compare 4/5 co-operate
  - Free-run timer 7 and output compare 6/7 co-operate

- LIN-USART (LIN=Local Interconnect Network) : 7 channels / 4 channels in case of MD_3 = 1
  - Full-duplex double buffer system (4 ch with 16 byte RX/TX FIFO buffer each)
  - With parity/without parity selectable
  - 1 or 2 stop bits selectable
  - 7 or 8 bits data length selectable
  - NRZ type transfer format
  - Asynchronous /synchronous communications selectable
    - USART channel 0 only for asynchronous communication
  - Master-slave communication function (multiprocessor mode)
  - Dedicated baud rate prescaler is embedded in each channel
  - External clock is able to use as transfer clock
  - Parity error, frame error, and overrun error detecting functions
  - SPI compatible
  - LIN master and slave
  - LIN-USART 0 and ICU 0 co-operate (for LIN sync field in slave mode)
  - LIN USART 2 and ICU 2 co-operate (for LIN sync field in slave mode)
  - LIN USART 3 and ICU 3 co-operate (for LIN sync field in slave mode)
  - LIN USART 4 and ICU 4 co-operate (for LIN sync field in slave mode)
  - LIN USART 5 and ICU 5 co-operate (for LIN sync field in slave mode)
  - LIN USART 6 and ICU 6 co-operate (for LIN sync field in slave mode)
  - LIN USART 7 and ICU 7 co-operate (for LIN sync field in slave mode)

- CAN : 6 channels
  - Supports CAN protocol version 2.0 part A and B
  - Bit rates up to 1 Mbit/s
  - 32 message objects, 1 channel with 64 message objects is under discussion
  - Each message object has its own identifier mask
  - Programmable FIFO mode (concatenation of message objects)
  - Maskable interrupt
  - Disabled Automatic Retransmission mode for Time Triggered CAN applications
  - Programmable loop-back mode for self-test operation

- I^2C (400k fast mode) : 2 channels
  - Master or slave transmission
  - Arbitration function
  - Clock synchronization function
  - Slave address and general call address detect function
  - Transfer direction detect function
  - Start condition repeat generation and detection function
  - Bus error detect function
  - Compatible to I2C standard and fast mode specification (operation up to 400 kHz, 10 bit addressing)
  - Includes clock divider functionality
  - SCL and SDA lines include optional noise filter. The noise filter allows the suppression of spikes in the range of 1 to 1.5 cycles of the Peripheral Clock.

- Sound Generator : 1 channel
  - 8-bit PWM signal is mixed with tone frequency from 16-bit reload counter
  - PWM clock by internal prescaler: $f_{RES}/2^0$, $f_{RES}/2^1$, $f_{RES}/2^2$, $f_{RES}/2^3$, $f_{RES}/2^4$
  - Tone frequency: PWM frequency / 2 / (reload value + 1)

- Time base/watchdog timer (26 bits)
  - Adjustable watchdog timer interval (between 2^{20} and 2^{26} system clock cycles)

- Real-time clock (counts during stop mode)
  - RTC module can be clocked either from 32 kHz quartz, 4 MHz quartz or from the RC Oscillator
  - Facility to correct oscillation deviation (subclock calibration)
  - Read/write accessible second/minute/ hour registers
  - Can signal interrupts every half second/second/ minute/hour/day
  - Internal clock divider and prescaler provide exact 1s clock based on a 4 MHz or a 32 kHz clock input
  - Prescaler value for 4 MHz is $1E847F_H$
  - Prescaler value for 32 kHz is $003FFF_H$

- Clock supervisor
  - Monitors external 32kHz and 4MHz for fails (e.g. crystal breaks)Switches in case of fail to an available recovery clock (other oscillator, or RC oscillator)

- Clock modulator
  - Reduction of Electro Magnetic Emission (EME)

- Subclock calibration
  - Calibration of the RTC timer in 32 kHz or RC oscillator operation, based on the more accurate 4 MHz quartz is possible

- Main oscillation stabilization timer
  - 23 bit counter for main oscillation stabilization wait when running in sub clock mode
  - Generates an interrupt when stabilization time has elapsed

- Sub oscillation stabilization timer
  - 15 bit counter for sub oscillation stabilization wait when running in main clock mode
  - Generates an interrupt when stabilization time has elapsed

2.4 Embedded Program/Data Memory

2.4.1 Flash features

- MB91F467BA : 1024 Kbyte + 64 Kbyte Flash
- MB91F466BA : 768 Kbyte + 64 Kbyte Flash
- MB91F465BA : 512 Kbyte + 32 Kbyte Flash
- MB91F464BA : 384 Kbyte + 32 Kbyte Flash
- Power: Single +3.0-5.5V supply
- Programmable wait state for read/write access
- Flash security with security vector at 0x0014:8000 – 0x0014:800F[1]
- Basic specification: Same as MBM29LV400TC (except size and part of sector configuration)
- Operation modes:
  - (1) 64-bit CPU mode:
    - CPU reads and executes programs in word (32-bit) length units.
    - Flash writing is not possible.
    - Actual Flash Memory access is performed in d-word (64-bit) length units.
  - (2) 32-bit CPU mode:
    - CPU reads, writes and executes programs in word (32-bit) length units.
    - Actual Flash Memory access is performed in word (32-bit) length units.
  - (3) 16-bit CPU mode:
    - CPU reads and writes in half-word (16-bit) length units.
    - Program execution from the Flash is not possible.
    - Actual Flash Memory access is performed in word (16-bit) length units.
  - (4) Flash memory mode (external access to Flash memory enabled)
- Features (through combination of Flash memory macro and FR-CPU interface circuit):
  - Functions as CPU program/data storage memory.
  - Enables access to 16/32/64-bit bus width.
  - Enables read/write/erase by CPU (auto program algorithm*).
  - Functions equivalent to MBM29LV400TC stand-alone Flash-memory product.
  - Enables read/write/erase by parallel Flash programmer (auto program algorithm*).

    *: Auto program algorithm = Embedded Algorithm TM

[1] See MB91460 hardware manual for further details.

2.4.2 CPU Mode

2.4.2.1 Flash configuration in CPU mode

Flash memory map in CPU mode (MD[2:0] = 00x):

MB91F467BA Flash memory map in CPU mode (MD[2:0]=00x)

addr								
0014:FFFFh 0014:C000h	SA6(8KB)				SA7(8KB)			
0014:BFFFh 0014:8000h	SA4(8KB)				SA5(8KB)			
0014:7FFFh 0014:4000h	SA2(8KB)				SA3(8KB)			
0014:3FFFh 0014:0000h	SA0(8KB)				SA1(8KB)			
0013:FFFFh 0012:0000h	SA22(64KB)				SA23(64KB)			
0011:FFFFh 0010:0000h	SA20(64KB)				SA21(64KB)			
000F:FFFFh 000E:0000h	SA18(64KB)				SA19(64KB)			
000D:FFFFh 000C:0000h	SA16(64KB)				SA17(64KB)			
000B:FFFFh 000A:0000h	SA14(64KB)				SA15(64KB)			
0009:FFFFh 0008:0000h	SA12(64KB)				SA13(64KB)			
0007:FFFFh 0006:0000h	SA10(64KB)				SA11(64KB)			
0005:FFFFh 0004:0000h	SA8(64KB)				SA9(64KB)			
	addr+0	addr+1	addr+2	addr+3	addr+4	addr+5	addr+6	addr+7
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]	
32bit read/write	dat[31:0]				dat[31:0]			

MB91F466BA Flash memory map in CPU mode (MD[2:0]=00x)

addr								
0014:FFFFh 0014:C000h	SA6(8KB)				SA7(8KB)			
0014:BFFFh 0014:8000h	SA4(8KB)				SA5(8KB)			
0014:7FFFh 0014:4000h	SA2(8KB)				SA3(8KB)			
0014:3FFFh 0014:0000h	SA0(8KB)				SA1(8KB)			
0013:FFFFh 0012:0000h	SA22(64KB)				SA23(64KB)			
0011:FFFFh 0010:0000h	SA20(64KB)				SA21(64KB)			
000F:FFFFh 000E:0000h	SA18(64KB)				SA19(64KB)			
000D:FFFFh 000C:0000h	SA16(64KB)				SA17(64KB)			
000B:FFFFh 000A:0000h	SA14(64KB)				SA15(64KB)			
0009:FFFFh 0008:0000h	SA12(64KB)				SA13(64KB)			
0007:FFFFh 0006:0000h	SA10(64KB)				SA11(64KB)			
0005:FFFFh 0004:0000h	SA8(64KB)				SA9(64KB)			
	addr+0	addr+1	addr+2	addr+3	addr+4	addr+5	addr+6	addr+7
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]	
32bit read	dat[31:0]				dat[31:0]			

Legend	
	Memory available in this area
	Memory not available in this area

MB91F465BA Flash memory map in CPU mode (MD[2:0]=00x)

addr								
0014:FFFFh 0014:C000h	SA6(8KB)				SA7(8KB)			
0014:BFFFh 0014:8000h	SA4(8KB)				SA5(8KB)			
0014:7FFFh 0014:4000h	SA2(8KB)				SA3(8KB)			
0014:3FFFh 0014:0000h	SA0(8KB)				SA1(8KB)			
0013:FFFFh 0012:0000h	SA22(64KB)				SA23(64KB)			
0011:FFFFh 0010:0000h	SA20(64KB)				SA21(64KB)			
000F:FFFFh 000E:0000h	SA18(64KB)				SA19(64KB)			
000D:FFFFh 000C:0000h	SA16(64KB)				SA17(64KB)			
000B:FFFFh 000A:0000h	SA14(64KB)				SA15(64KB)			
0009:FFFFh 0008:0000h	SA12(64KB)				SA13(64KB)			
0007:FFFFh 0006:0000h	SA10(64KB)				SA11(64KB)			
0005:FFFFh 0004:0000h	SA8(64KB)				SA9(64KB)			
	addr+0	addr+1	addr+2	addr+3	addr+4	addr+5	addr+6	addr+7
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]	
32bit read	dat[31:0]				dat[31:0]			

Legend: Memory available in this area

Memory not available in this area

MB91F464BA Flash memory map in CPU mode (MD[2:0]=00x)

addr								
0014:FFFFh 0014:C000h	SA6(8KB)				SA7(8KB)			
0014:BFFFh 0014:8000h	SA4(8KB)				SA5(8KB)			
0014:7FFFh 0014:4000h	SA2(8KB)				SA3(8KB)			
0014:3FFFh 0014:0000h	SA0(8KB)				SA1(8KB)			
0013:FFFFh 0012:0000h	SA22(64KB)				SA23(64KB)			
0011:FFFFh 0010:0000h	SA20(64KB)				SA21(64KB)			
000F:FFFFh 000E:0000h	SA18(64KB)				SA19(64KB)			
000D:FFFFh 000C:0000h	SA16(64KB)				SA17(64KB)			
000B:FFFFh 000A:0000h	SA14(64KB)				SA15(64KB)			
0009:FFFFh 0008:0000h	SA12(64KB)				SA13(64KB)			
0007:FFFFh 0006:0000h	SA10(64KB)				SA11(64KB)			
0005:FFFFh 0004:0000h	SA8(64KB)				SA9(64KB)			
	addr+0	addr+1	addr+2	addr+3	addr+4	addr+5	addr+6	addr+7
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]	
32bit read	dat[31:0]				dat[31:0]			

Legend: Memory available in this area

Memory not available in this area

2.4.2.2 Flash access timing settings in CPU mode

The Flash access timing settings described below are valid for MB91F467BA/466BA/465BA/464BA in the 1.8V operation mode of the Main regulator and Flash[2].

The following tables list all settings for a given maximum Core Frequency (through the setting of CLKB or maximum clock modulation) for Flash read and write access.

Flash read timing settings for MB91F467BA/466BA/465BA/464BA

Core clock (CLKB)	ATD	ALEH	EQ	WEXH	WTC
to 24 MHz	0	0	0	-	1
to 48 MHz	0	0	1	-	2
to 96 MHz	1	1	3	-	4

Flash write timing settings for MB91F467BA/466BA/465BA/464BA (synchronous write)

Core clock (CLKB)	ATD	ALEH	EQ	WEXH	WTC
to 16 MHz	0	-	-	0	3
to 32 MHz	0	-	-	0	4
to 48 MHz	0	-	-	0	5
to 64 MHz	1	-	-	0	6
to 96 MHz	1	-	-	0	7

[2] Keep REGSEL_FLASHSEL=0 and REGSEL_MAINSEL=0 at their initial value (HWM Chapter 52.3.1)

2.4.2.3 Address mapping from CPU to parallel programming mode

8kB Sectors (SA0 – SA7)

SA0, SA2, SA4, SA6:

Condition: addr >= 14:0000h && addr <= 14:FFFFh && addr[2]==0 :

FA := addr - addr%00:4000h + (addr%00:4000h)/2 - (addr/2)%4 + addr%4 - 05:0000h

SA1, SA3, SA5, SA7:

Condition: addr >= 14:0000h && addr <= 14:FFFFh && addr[2]==1:

FA := addr - addr%00:4000h + (addr%00:4000h)/2 + 00:2000h - (addr/2)%4 + addr%4 - 05:0000h

64kB Sectors (SA8 – SA23)

SA8, SA10, SA12, SA14, SA16, SA18, SA20, SA22:

Condition: addr >= 04:0000h && addr <= 13:FFFFh && addr[2]==0:

FA := addr - addr%02:0000 + (addr%02:0000h)/2 - (addr/2)%4 + addr%4 + 0C:0000h

SA9, SA11, SA13, SA15, SA17, SA19, SA21, SA23:

Condition: addr >= 04:0000h && addr <= 13:FFFFh && addr[2]==1:

FA := addr - addr%02:0000h + (addr%02:0000h)/2 + 01:0000h - (addr/2)%4 + addr%4 + 0C:0000h

Remark: FA result is without 20:0000h offset for parallel flash programming[3].

[3] Set offset by keeping FA[21] = 1 as described in section 2.4.3.

2.4.3 Parallel flash programming mode

2.4.3.1 Flash configuration in parallel flash programming mode

Parallel Flash programming mode (MD[2:0] = 111):

FA[21:0]	
003F:FFFFh 003F:0000h	SA23(64KB)
003E:FFFFh 003E:0000h	SA22(64KB)
003D:FFFFh 003D:0000h	SA21(64KB)
003C:FFFFh 003C:0000h	SA20(64KB)
003B:FFFFh 003B:0000h	SA19(64KB)
003A:FFFFh 003A:0000h	SA18(64KB)
0039:FFFFh 0039:0000h	SA17(64KB)
0038:FFFFh 0038:0000h	SA16(64KB)
0037:FFFFh 0037:0000h	SA15(64KB)
0036:FFFFh 0036:0000h	SA14(64KB)
0035:FFFFh 0035:0000h	SA13(64KB)
0034:FFFFh 0034:0000h	SA12(64KB)
0033:FFFFh 0033:0000h	SA11(64KB)
0032:FFFFh 0032:0000h	SA10(64KB)
0031:FFFFh 0031:0000h	SA9(64KB)
0030:FFFFh 0030:0000h	SA8(64KB)
002F:FFFFh 002F:E000h	SA7(8KB)
002F:DFFFh 002F:C000h	SA6(8KB)
002F:BFFFh 002F:A000h	SA5(8KB)
002F:9FFFh 002F:8000h	SA4(8KB)
002F:7FFFh 002F:6000h	SA3(8KB)
002F:5FFFh 002F:4000h	SA2(8KB)
002F:3FFFh 002F:2000h	SA1(8KB)
002F:1FFFh 002F:0000h	SA0(8KB)

	FA[1:0]=00	FA[1:0]=10
16bit write mode	DQ[15:0]	DQ[15:0]

Remark: Always keep FA[0] = 0 and FA[21] = 1 in parallel programming mode.

2.4.3.2 Pin connections in parallel programming mode

Resetting after setting the MD[2:0] pins to [111] will halt CPU functioning. At this time, the Flash memory's interface circuit enables direct control of the Flash memory unit from external pins by directly linking some of the signals to GP-Ports. Please see table below for signal mapping.

In this mode, the Flash memory appears to the external pins as a stand-alone unit. This mode is generally set when writing/erasing using the parallel Flash programmer. In this mode, all operations of the 8.5 Mbits Flash memory's Auto Algorithms are available.

Correspondence between MBM29LV400TC and Flash Memory Control Signals

MBM29LV400TC External pins	FR-CPU mode	MB91F467BA external pins			Comment
		Flash memory mode	Normal function	Pin number	
-	INITX	-	INITX	84	
RESET	-	FRSTX	GP16_6	70	
-	-	MD2	MD2	76	Set to '1'
-	-	MD1	MD1	75	Set to '1'
-	-	MD0	MD0	74	Set to '1'
RY/BY	FMCS:RDY bit	RY/BYX	GP18_2	100	
BYTE	Internally fixed to 'H'	BYTEX	GP16_4	68	
WE	Internal control signal + control via interface circuit	WEX	GP16_7	71	
OE		OEX	GP07_7	3	
CE		CEX	GP07_6	2	
-		ATDIN	GP18_6	103	Set to '0'
-		EQIN	GP18_5	102	Set to '0'
-		TESTX	GP16_5	69	Set to '1'
-		RDYI	GP18_4	101	Set to '0'
A-1	Internal address bus	FA0	GP05_5	17	Set to '0'
A0 to A3		FA1 to FA4	GP19_0 to GP19_2, GP19_4	92 to 95	
A4 to A7		FA5 to FA8	GP19_5 to GP19_6, GP18_0 to GP18_1	96 to 99	
A8 to A11		FA9 to FA12	GP06_0 to GP06_3	4 to 7	
A12 to A15		FA13 to FA16	GP06_4 to GP06_7	8 to 11	
A16 to A19		FA17 to FA20	GP05_0 to GP05_3	12 to 15	
-		FA21	GP05_4	16	Set to '1'
DQ0 to DQ7	Internal data bus	DQ0 to DQ7	GP00_0 to GP00_7	28 to 35	
DQ8 to DQ15		DQ8 to DQ15	GP01_0 to GP01_7	20 to 27	

2.4.4 Flash Security

2.4.4.1 Vector addresses

Two Flash Security Vectors (FSV1, FSV2) are located parallel to the Boot Security Vectors (BSV1, BSV2) controlling the protection functions of the flash security module:

FSV1: 0x14:8000 **BSV1: 0x14:8004**

FSV2: 0x14:8008 **BSV2: 0x14:800C**

2.4.4.2 Security Vector FSV1

The setting of the Flash Security Vector FSV1 is responsible for the read and write protection modes and the individual write protection of the 8 kB sectors.

■ **FSV1 (bits 31 to 16)**

The setting of the Flash Security Vector FSV1 bits [31:16] is responsible for the read and write protection modes.

Explanation of the bits in the Flash Security Vector FSV1[31:16]

FSV1[31:19]	FSV1[18] Write Protection Level	FSV1[17] Write Protection	FSV1[16] Read Protection	Flash Security Mode
set all to ‘0’	set to ‘0’	set to ‘0’	set to ‘1’	Read Protection (all device modes, except INTVEC mode MD[2:0]=”000”)
set all to ‘0’	set to ‘0’	set to ‘1’	set to ‘0’	Write Protection (all device modes, without exception)
set all to ‘0’	set to ‘0’	set to ‘1’	set to ‘1’	Read Protection (all device modes, except INTVEC mode MD[2:0]=”000”) and Write Protection (all device modes)
set all to ‘0’	set to ‘1’	set to ‘0’	set to ‘1’	Read Protection (all device modes, except INTVEC mode MD[2:0]=”000”)
set all to ‘0’	set to ‘1’	set to ‘1’	set to ‘0’	Write Protection (all device modes, except INTVEC mode MD[2:0]=”000”)
set all to ‘0’	set to ‘1’	set to ‘1’	set to ‘1’	Read Protection (all device modes, except INTVEC mode MD[2:0]=”000”) and Write Protection (all device modes except INTVEC mode MD[2:0]=”000”)

■ **FSV1 (bits 15 to 0)**

The setting of the Flash Security Vector FSV1 bits [15:0] is responsible for the individual write protection of the 8 kB sectors. It is only evaluated if write protection bit FSV1[17] is set.

Explanation of the bits in the Flash Security Vector FSV1[15:0]

FSV1 bit	Sector	Enable Write Protection	Disable Write Protection	Comment
FSV1[0]	SA0	set to '0'	set to '1'	
FSV1[1]	SA1	set to '0'	set to '1'	
FSV1[2]	SA2	set to '0'	set to '1'	
FSV1[3]	SA3	set to '0'	set to '1'	
FSV1[4]	SA4	set to '0'	-	**Write protection is mandatory!**
FSV1[5]	SA5	set to '0'	set to '1'	
FSV1[6]	SA6	set to '0'	set to '1'	
FSV1[7]	SA7	set to '0'	set to '1'	
FSV1[8]	-	set to '0'	set to '1'	not available
FSV1[9]	-	set to '0'	set to '1'	not available
FSV1[10]	-	set to '0'	set to '1'	not available
FSV1[11]	-	set to '0'	set to '1'	not available
FSV1[12]	-	set to '0'	set to '1'	not available
FSV1[13]	-	set to '0'	set to '1'	not available
FSV1[14]	-	set to '0'	set to '1'	not available
FSV1[15]	-	set to '0'	set to '1'	not available

Remark: It is mandatory to always set the sector where the Flash Security Vectors FSV1 and FSV2 are located to write protected (here sector SA4). Otherwise it is possible to overwrite the Security Vector to a setting where it is possible to either read out the flash content or manipulate data by writing.

See section 2.4.2.1 for an overview about the sector organisation of the Flash Memory.

2.4.4.3 Security Vector FSV2

The setting of the Flash Security Vector FSV2 bits [31:0] is responsible for the individual write protection of the 64 kB sectors. It is only evaluated if write protection bit FSV1[17] is set.

Explanation of the bits in the Flash Security Vector FSV2[31:0]

FSV1 bit	Sector	Enable Write Protection	Disable Write Protection	Comment
FSV2[0]	SA8	set to ‘0’	set to ‘1’	
FSV2[1]	SA9	set to ‘0’	set to ‘1’	
FSV2[2]	SA10	set to ‘0’	set to ‘1’	
FSV2[3]	SA11	set to ‘0’	set to ‘1’	
FSV2[4]	SA12	set to ‘0’	set to ‘1’	
FSV2[5]	SA13	set to ‘0’	set to ‘1’	
FSV2[6]	SA14	set to ‘0’	set to ‘1’	
FSV2[7]	SA15	set to ‘0’	set to ‘1’	
FSV2[8]	SA16	set to ‘0’	set to ‘1’	
FSV2[9]	SA17	set to ‘0’	set to ‘1’	
FSV2[10]	SA18	set to ‘0’	set to ‘1’	
FSV2[11]	SA19	set to ‘0’	set to ‘1’	
FSV2[12]	SA20	set to ‘0’	set to ‘1’	
FSV2[13]	SA21	set to ‘0’	set to ‘1’	
FSV2[14]	SA22	set to ‘0’	set to ‘1’	
FSV2[15]	SA8	set to ‘0’	set to ‘1’	
FSV2[16]	SA9	set to ‘0’	set to ‘1’	not available
FSV2[17]	SA10	set to ‘0’	set to ‘1’	not available
FSV2[18]	SA11	set to ‘0’	set to ‘1’	not available
FSV2[19]	SA12	set to ‘0’	set to ‘1’	not available
FSV2[20]	SA13	set to ‘0’	set to ‘1’	not available
FSV2[21]	SA14	set to ‘0’	set to ‘1’	not available

FSV2[22]	SA15	set to ‘0’	set to ‘1’	not available
FSV2[23]	SA16	set to ‘0’	set to ‘1’	not available
FSV2[24]	SA17	set to ‘0’	set to ‘1’	not available
FSV2[25]	SA18	set to ‘0’	set to ‘1’	not available
FSV2[26]	SA19	set to ‘0’	set to ‘1’	not available
FSV2[27]	SA20	set to ‘0’	set to ‘1’	not available
FSV2[28]	SA21	set to ‘0’	set to ‘1’	not available
FSV2[29]	SA22	set to ‘0’	set to ‘1’	not available
FSV2[30]	SA23	set to ‘0’	set to ‘1’	not available
FSV2[31]	SA23	set to ‘0’	set to ‘1’	not available

See section 2.4.2.1 for an overview about the sector organisation of the Flash Memory.

2.4.4.4 Register description for Flash Security

For a description of Flash Security registers please refer to Hardware Manual chapter 55.

3 Recommended Settings

3.1 PLL and Clockgear settings

Please note that for MB91F467BA/466BA/465BA/464BA the core base clock frequencies are valid in the 1.8V operation mode of the Main regulator and Flash[4].

Recommended PLL divider and clockgear settings

PLL Input (CK) [MHz]	Frequency Parameter		Clockgear Parameter		PLL Output (X) [MHz]	Core base Clock [MHz]
	DIVM	DIVN	DIVG	MULG		
4	2	24	16	24	192	96
4	2	23	16	24	184	92
4	2	22	16	24	176	88
4	2	21	16	20	168	84
4	2	20	16	20	160	80
4	2	19	16	20	152	76
4	2	18	16	20	144	72
4	2	17	16	16	136	68
4	2	16	16	16	128	64
4	2	15	16	16	120	60
4	2	14	16	16	112	56
4	2	13	16	12	104	52
4	2	12	16	12	96	48
4	2	11	16	12	88	44
4	4	10	16	24	160	40
4	4	9	16	24	144	36
4	4	8	16	24	128	32
4	4	7	16	24	112	28

[4] Keep REGSEL_FLASHSEL=0 and REGSEL_MAINSEL=0 at their initial value (HWM Chapter 52.3.1)

4	6	6	16	24	144	24
4	8	5	16	28	160	20
4	10	4	16	32	160	16
4	12	3	16	32	144	12

3.2 Flash interface settings

Please refer to section 2.4.2.2 ‘Flash access timing settings in CPU mode’ for the recommended Flash interface settings.

3.3 Clock Modulator settings

The following table shows all possible settings for the Clock Modulator in a base clock frequency range from 32MHz up to 84MHz. Fmax must not exceed the maximum specified frequency of 96MHz.

The flash access time settings (see section 2.4.2.2) need to be adjusted according to Fmax while the PLL and clockgear settings (see section 3.1) should be set according to base clock frequency.

Clock Modulator settings and frequency range

Modulation Degree	Random No	CMPR	Baseclk	Fmin	Fmax
(k)	(N)	[hex]	[MHz]	[MHz]	[MHz]
1	3	026F	84	76.1	93.8
1	3	026F	80	72.6	89.1
1	5	02AE	80	68.7	95.8
2	3	046E	80	68.7	95.8
1	3	026F	76	69.1	84.5
1	5	02AE	76	65.3	90.8
2	3	046E	76	65.3	90.8
1	3	026F	72	65.5	79.9
1	5	02AE	72	62	85.8
1	7	02ED	72	58.8	92.7
2	3	046E	72	62	85.8
3	3	066D	72	58.8	92.7
1	3	026F	68	62	75.3
1	5	02AE	68	58.7	80.9
1	7	02ED	68	55.7	87.3
1	9	032C	68	53	95
2	3	046E	68	58.7	80.9
2	5	04AC	68	53	95
3	3	066D	68	55.7	87.3
4	3	086C	68	53	95
1	3	026F	64	58.5	70.7
1	5	02AE	64	55.3	75.9
1	7	02ED	64	52.5	82
1	9	032C	64	49.9	89.1
2	3	046E	64	55.3	75.9
2	5	04AC	64	49.9	89.1
3	3	066D	64	52.5	82
4	3	086C	64	49.9	89.1
1	3	026F	60	54.9	66.1
1	5	02AE	60	51.9	71
1	7	02ED	60	49.3	76.7
1	9	032C	60	46.9	83.3
1	11	036B	60	44.7	91.3
2	3	046E	60	51.9	71
2	5	04AC	60	46.9	83.3

Modulation Degree	Random No	CMPR	Baseclk	Fmin	Fmax
(k)	(N)	[hex]	[MHz]	[MHz]	[MHz]
3	3	066D	60	49.3	76.7
4	3	086C	60	46.9	83.3
5	3	0A6B	60	44.7	91.3
1	3	026F	56	51.4	61.6
1	5	02AE	56	48.6	66.1
1	7	02ED	56	46.1	71.4
1	9	032C	56	43.8	77.6
1	11	036B	56	41.8	84.9
1	13	03AA	56	39.9	93.8
2	3	046E	56	48.6	66.1
2	5	04AC	56	43.8	77.6
2	7	04EA	56	39.9	93.8
3	3	066D	56	46.1	71.4
3	5	06AA	56	39.9	93.8
4	3	086C	56	43.8	77.6
5	3	0A6B	56	41.8	84.9
6	3	0C6A	56	39.9	93.8
1	3	026F	52	47.8	57
1	5	02AE	52	45.2	61.2
1	7	02ED	52	42.9	66.1
1	9	032C	52	40.8	71.8
1	11	036B	52	38.8	78.6
1	13	03AA	52	37.1	86.8
2	3	046E	52	45.2	61.2
2	5	04AC	52	40.8	71.8
2	7	04EA	52	37.1	86.8
3	3	066D	52	42.9	66.1
3	5	06AA	52	37.1	86.8
4	3	086C	52	40.8	71.8
5	3	0A6B	52	38.8	78.6
6	3	0C6A	52	37.1	86.8
1	3	026F	48	44.2	52.5
1	5	02AE	48	41.8	56.4
1	7	02ED	48	39.6	60.9
1	9	032C	48	37.7	66.1
1	11	036B	48	35.9	72.3
1	13	03AA	48	34.3	79.9
1	15	03E9	48	32.8	89.1
2	3	046E	48	41.8	56.4
2	5	04AC	48	37.7	66.1
2	7	04EA	48	34.3	79.9
3	3	066D	48	39.6	60.9
3	5	06AA	48	34.3	79.9
4	3	086C	48	37.7	66.1
5	3	0A6B	48	35.9	72.3
6	3	0C6A	48	34.3	79.9

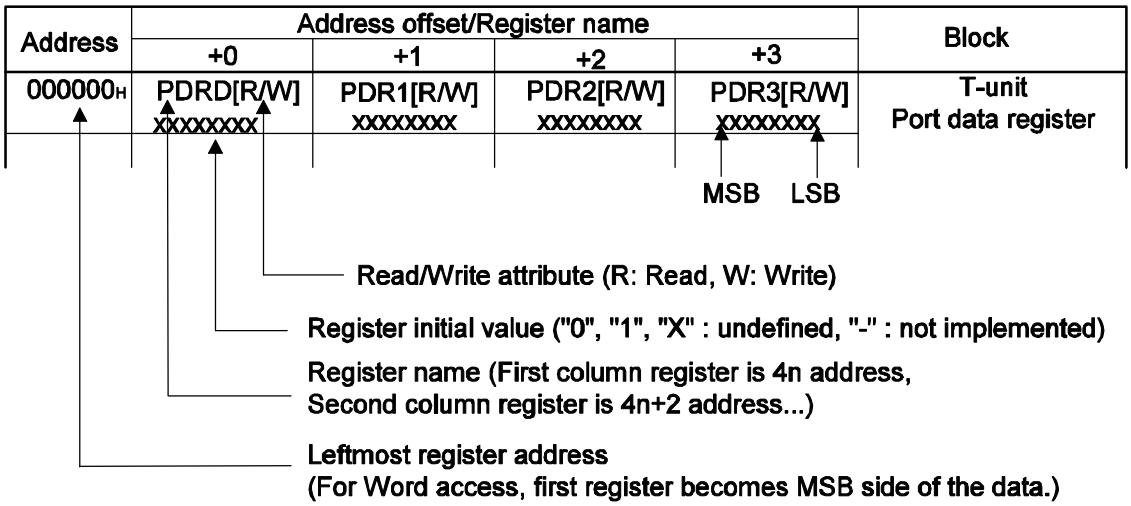
Modulation Degree	Random No	CMPR	Baseclk	Fmin	Fmax
(k)	(N)	[hex]	[MHz]	[MHz]	[MHz]
7	3	0E69	48	32.8	89.1
1	3	026F	44	40.6	48.1
1	5	02AE	44	38.4	51.6
1	7	02ED	44	36.4	55.7
1	9	032C	44	34.6	60.4
1	11	036B	44	33	66.1
1	13	03AA	44	31.5	73
1	15	03E9	44	30.1	81.4
2	3	046E	44	38.4	51.6
2	5	04AC	44	34.6	60.4
2	7	04EA	44	31.5	73
2	9	0528	44	28.9	92.1
3	3	066D	44	36.4	55.7
3	5	06AA	44	31.5	73
4	3	086C	44	34.6	60.4
4	5	08A8	44	28.9	92.1
5	3	0A6B	44	33	66.1
6	3	0C6A	44	31.5	73
7	3	0E69	44	30.1	81.4
8	3	1068	44	28.9	92.1
1	3	026F	40	37	43.6
1	5	02AE	40	34.9	46.8
1	7	02ED	40	33.1	50.5
1	9	032C	40	31.5	54.8
1	11	036B	40	30	59.9
1	13	03AA	40	28.7	66.1
1	15	03E9	40	27.4	73.7
2	3	046E	40	34.9	46.8
2	5	04AC	40	31.5	54.8
2	7	04EA	40	28.7	66.1
2	9	0528	40	26.3	83.3
3	3	066D	40	33.1	50.5
3	5	06AA	40	28.7	66.1
3	7	06E7	40	25.3	95.8
4	3	086C	40	31.5	54.8
4	5	08A8	40	26.3	83.3
5	3	0A6B	40	30	59.9
6	3	0C6A	40	28.7	66.1
7	3	0E69	40	27.4	73.7
8	3	1068	40	26.3	83.3
9	3	1267	40	25.3	95.8
1	3	026F	36	33.3	39.2
1	5	02AE	36	31.5	42
1	7	02ED	36	29.9	45.3
1	9	032C	36	28.4	49.2
1	11	036B	36	27.1	53.8

Modulation Degree	Random No	CMPR	Baseclk	Fmin	Fmax
(k)	(N)	[hex]	[MHz]	[MHz]	[MHz]
1	13	03AA	36	25.8	59.3
1	15	03E9	36	24.7	66.1
2	3	046E	36	31.5	42
2	5	04AC	36	28.4	49.2
2	7	04EA	36	25.8	59.3
2	9	0528	36	23.7	74.7
3	3	066D	36	29.9	45.3
3	5	06AA	36	25.8	59.3
3	7	06E7	36	22.8	85.8
4	3	086C	36	28.4	49.2
4	5	08A8	36	23.7	74.7
5	3	0A6B	36	27.1	53.8
6	3	0C6A	36	25.8	59.3
7	3	0E69	36	24.7	66.1
8	3	1068	36	23.7	74.7
9	3	1267	36	22.8	85.8
1	3	026F	32	29.7	34.7
1	5	02AE	32	28	37.3
1	7	02ED	32	26.6	40.2
1	9	032C	32	25.3	43.6
1	11	036B	32	24.1	47.7
1	13	03AA	32	23	52.5
1	15	03E9	32	22	58.6
2	3	046E	32	28	37.3
2	5	04AC	32	25.3	43.6
2	7	04EA	32	23	52.5
2	9	0528	32	21.1	66.1
2	11	0566	32	19.5	89.1
3	3	066D	32	26.6	40.2
3	5	06AA	32	23	52.5
3	7	06E7	32	20.3	75.9
4	3	086C	32	25.3	43.6
4	5	08A8	32	21.1	66.1
5	3	0A6B	32	24.1	47.7
5	5	0AA6	32	19.5	89.1
6	3	0C6A	32	23	52.5
7	3	0E69	32	22	58.6
8	3	1068	32	21.1	66.1
9	3	1267	32	20.3	75.9
10	3	1466	32	19.5	89.1

4 IO Map

This section shows the association between memory space and each register of peripheral resources.

• Table convention



Note: Bit value of register shows initial values as follows.

- "1": Initial value is "1".
- "0": Initial value is "0".
- "X": Initial value is indeterminate.
- "N/A": No physical register exists in the position.

Do not use other data access attributes to access data.

Address	Register				Block
	+0	+1	+2	+3	
000000_H	PDR00 [R/W] XXXXXXXX	PDR01 [R/W] XXXXXXXX	~~PDR02 [R/W]~~ ~~XXXXXXXX~~	~~PDR03 [R/W]~~ ~~XXXXXXXX~~	R-bus Port Data Register
000004_H	~~PDR04 [R/W]~~ ~~XXXXXXXX~~	PDR05 [R/W] - - XXXXXX	PDR06 [R/W] XXXXXXXX	PDR07 [R/W] XXXXXXXX	
000008_H	PDR08 [R/W] X - - X - - - X	PDR09 [R/W] - - - - - - XX	PDR10 [R/W] - - - - - - - X	~~PDR11 [R/W]~~ ~~XXXXXXXX~~	
$00000C_H$	~~PDR12 [R/W]~~ ~~XXXXXXXX~~	~~PDR13 [R/W]~~ ~~XXXXXXXX~~	PDR14 [R/W] XXXXXXXX	PDR15 [R/W] XXXXXXXX	
000010_H	PDR16 [R/W] XXXXXXXX	PDR17 [R/W] XXXXXXXX	PDR18 [R/W] - XXX - XXX	PDR19 [R/W] - XXX - XXX	
000014_H	PDR20 [R/W] - XXX - XXX	PDR21 [R/W] - - - - - - XX	PDR22 [R/W] XXXXXXXX	PDR23 [R/W] XXXXXXXX	
000018_H	PDR24 [R/W] XXXXXXXX	~~PDR25 [R/W]~~ ~~XXXXXXXX~~	PDR26 [R/W] XXXXXXXX	PDR27 [R/W] XXXXXXXX	
$00001C_H$	PDR28 [R/W] XXXXXXXX	PDR29 [R/W] XXXXXXXX	~~PDR30 [R/W]~~ ~~XXXXXXXX~~	~~PDR31 [R/W]~~ ~~XXXXXXXX~~	
000020_H	~~PDR32 [R/W]~~ ~~XXXXXXXX~~	~~PDR33 [R/W]~~ ~~XXXXXXXX~~	~~PDR34 [R/W]~~ ~~XXXXXXXX~~	~~PDR35 [R/W]~~ ~~XXXXXXXX~~	
000024_H - $00002C_H$	reserved				(do not use)
000030_H	EIRR0 [R/W]] *3 00000000:MD3=0 11110000:MD3=1	ENIR0 [R/W] 00000000	ELVR0 [R/W]] *3 00000000 00000000		Ext. INT 0-7 NMI

Address	Register				Block
	+0	+1	+2	+3	
000034_H	EIRR1 [R/W]] *3 00000000	ENIR1 [R/W] 00000000	ELVR1 [R/W] *3 00000000 00000000		Ext. INT 8-15
000038_H	DICR [R/W] - - - - - - - 0	HRCL [R/W] 0 - - 11111	RBSYNC *1		DLYI/I-unit
$00003C_H$	reserved				(do not use)
000040_H	SCR00 [R/W,W] 00000000	SMR00 [R/W,W] 00000000	SSR00 [R/W,R] 00001000	RDR00/TDR00 [R/W] 00000000	USART (LIN) 0
000044_H	ESCR00 [R/W] 00000X00	ECCR00 [R/W,R,W] -00000XX	res.		
000048_H	~~SCR01 [R/W,W] 00000000~~	~~SMR01 [R/W,W] 00000000~~	~~SSR01 [R/W,R] 00001000~~	~~RDR01/TDR01 [R/W] 00000000~~	~~USART (LIN) 1~~
$00004C_H$	~~ESCR01 [R/W] 00000X00~~	~~ECCR01 [R/W,R,W] -00000XX~~	res.		
000050_H	SCR02 [R/W,W] 00000000	SMR02 [R/W,W] 00000000	SSR02 [R/W,R] 00001000	RDR02/TDR02 [R/W] 00000000	USART (LIN) 2
000054_H	ESCR02 [R/W] 00000X00	ECCR02 [R/W,R,W] -00000XX	res.		
000058_H	SCR03 [R/W,W] 00000000	SMR03 [R/W,W] 00000000	SSR03 [R/W,R] 00001000	RDR03/TDR03 [R/W] 00000000	USART (LIN) 3
$00005C_H$	ESCR03 [R/W] 00000X00	ECCR03 [R/W,R,W] -00000XX	res.		
000060_H	SCR04 [R/W,W] 00000000	SMR04 [R/W,W] 00000000	SSR04 [R/W,R] 00001000	RDR04/TDR04 [R/W] 00000000	USART (LIN) 4 with FIFO

Address	Register				Block
	+0	+1	+2	+3	
000064_H	ESCR04 [R/W] 00000X00	ECCR04 [R/W,R,W] -00000XX	FSR04 [R] - - - 00000	FCR04 [R/W] 0001 - 000	
000068_H	SCR05 [R/W,W] 00000000	SMR05 [R/W,W] 00000000	SSR05 [R/W,R] 00001000	RDR05/TDR05 [R/W] 00000000	USART (LIN) 5 with FIFO
$00006C_H$	ESCR05 [R/W] 00000X00	ECCR05 [R/W,R,W] -00000XX	FSR05 [R] - - - 00000	FCR05 [R/W] 0001 - 000	
000070_H	SCR06 [R/W,W] 00000000	SMR06 [R/W,W] 00000000	SSR06 [R/W,R] 00001000	RDR06/TDR06 [R/W] 00000000	USART (LIN) 6 with FIFO
000074_H	ESCR06 [R/W] 00000X00	ECCR06 [R/W,R,W] -00000XX	FSR06 [R] - - - 00000	FCR06 [R/W] 0001 - 000	
000078_H	SCR07 [R/W,W] 00000000	SMR07 [R/W,W] 00000000	SSR07 [R/W,R] 00001000	RDR07/TDR07 [R/W] ***00000000***	USART (LIN) 7 with FIFO
$00007C_H$	ESCR07 [R/W] 00000X00	ECCR07 [R/W,R,W] -00000XX	FSR07 [R] - - - 00000	FCR07 [R/W] 0001 - 000	
000080_H	BGR100 [R/W] 00000000	BGR000 [R/W] 00000000	~~BCR101 [R/W] 00000000~~	~~BCR001 [R/W] 00000000~~	***Baudrate Generator USART (LIN) 0-7***
000084_H	BGR102 [R/W] 00000000	BGR002 [R/W] 00000000	BGR103 [R/W] 00000000	BGR003 [R/W] 00000000	
000088_H	BGR104 [R/W] 00000000	BGR004 [R/W] 00000000	BGR105 [R/W] 00000000	BGR005 [R/W] 00000000	
$00008C_H$	BGR106 [R/W] 00000000	BGR006 [R/W] 00000000	BGR107 [R/W] 00000000	BGR007 [R/W] 00000000	
000090_H - $0000CC_H$	Reserved				

Address	Register				Block
	+0	+1	+2	+3	
$0000D0_H$	IBCR0 [R/W] 00000000	IBSR0 [R] 00000000	ITBAH0 [R/W] - - - - - - 00	ITBAL0 [R/W] 00000000	I2C 0
$0000D4_H$	ITMKH0 [R/W] 00 - - - - 11	ITMKL0 [R/W] 11111111	ISMK0 [R/W] 01111111	ISBA0 [R/W] - 0000000	
$0000D8_H$	res.	IDAR0 [R/W] 00000000	ICCR0 [R/W] - 0011111	res.	
$0000DC_H$	IBCR1 [R/W] 00000000	IBSR1 [R] 00000000	ITBAH1 [R/W] - - - - - - 00	ITBAL1 [R/W] 00000000	I2C 1
$0000E0_H$	ITMKH1 [R/W] 00 - - - - 11	ITMKL1 [R/W] 11111111	ISMK1 [R/W] 01111111	ISBA1 [R/W] - 0000000	
$0000E4_H$	res.	IDAR1 [R/W] 00000000	ICCR1 [R/W] - 0011111	res.	
$0000E8_H$ - $0000FC_H$	Reserved				
000100_H	GCN10 [R/W] 00110010 00010000		res.	GCN20 [R/W] - - - - 0000	PPG Control 0-3
000104_H	GCN11 [R/W] 00110010 00010000		res.	GCN21 [R/W] - - - - 0000	PPG Control 4-7
000108_H	GCN12 [R/W] 00110010 00010000		res.	GCN22 [R/W] - - - - 0000	PPG Control 8-11
000110_H	PTMR00 [R] 11111111 11111111		PCSR00 [W] XXXXXXXX XXXXXXXX		PPG 0

Address	Register				Block
	+0	+1	+2	+3	
000114_H	PDUT00 [W] XXXXXXXX XXXXXXXX		PCNH00 [R/W] 0000000 -	PCNL00 [R/W] 000000 - 0	
000118_H	PTMR01 [R] 11111111 11111111		PCSR01 [W] XXXXXXXX XXXXXXXX		PPG 1
$00011C_H$	PDUT01 [W] XXXXXXXX XXXXXXXX		PCNH01 [R/W] 0000000 -	PCNL01 [R/W] 000000 - 0	
000120_H	PTMR02 [R] 11111111 11111111		PCSR02 [W] XXXXXXXX XXXXXXXX		PPG 2
000124_H	PDUT02 [W] XXXXXXXX XXXXXXXX		PCNH02 [R/W] 0000000 -	PCNL02 [R/W] 000000 - 0	
000128_H	PTMR03 [R] 11111111 11111111		PCSR03 [W] XXXXXXXX XXXXXXXX		PPG 3
$00012C_H$	PDUT03 [W] XXXXXXXX XXXXXXXX		PCNH03 [R/W] 0000000 -	PCNL03 [R/W] 000000 - 0	
000130_H	PTMR04 [R] 11111111 11111111		PCSR04 [W] XXXXXXXX XXXXXXXX		PPG 4
000134_H	PDUT04 [W] XXXXXXXX XXXXXXXX		PCNH04 [R/W] 0000000 -	PCNL04 [R/W] 000000 - 0	
000138_H	PTMR05 [R] 11111111 11111111		PCSR05 [W] XXXXXXXX XXXXXXXX		PPG 5
$00013C_H$	PDUT05 [W] XXXXXXXX XXXXXXXX		PCNH05 [R/W] 0000000 -	PCNL05 [R/W] 000000 - 0	

Address	Register				Block
	+0	+1	+2	+3	
000140_H	PTMR06 [R] 11111111 11111111		PCSR06 [W] XXXXXXXX XXXXXXXX		PPG 6
000144_H	PDUT06 [W] XXXXXXXX XXXXXXXX		PCNH06 [R/W] 0000000 -	PCNL06 [R/W] 000000 - 0	
000148_H	PTMR07 [R] 11111111 11111111		PCSR07 [W] XXXXXXXX XXXXXXXX		PPG 7
$00014C_H$	PDUT07 [W] XXXXXXXX XXXXXXXX		PCNH07 [R/W] 0000000 -	PCNL07 [R/W] 000000 - 0	
000150_H	PTMR08 [R] 11111111 11111111		PCSR08 [W] XXXXXXXX XXXXXXXX		PPG 8
000154_H	PDUT08 [W] XXXXXXXX XXXXXXXX		PCNH08 [R/W] 0000000 -	PCNL08 [R/W] 000000 - 0	
000158_H	PTMR09 [R] 11111111 11111111		PCSR09 [W] XXXXXXXX XXXXXXXX		PPG 9
$00015C_H$	PDUT09 [W] XXXXXXXX XXXXXXXX		PCNH09 [R/W] 0000000 -	PCNL09 [R/W] 000000 - 0	
000160_H	PTMR10 [R] 11111111 11111111		PCSR10 [W] XXXXXXXX XXXXXXXX		PPG 10
000164_H	PDUT10 [W] XXXXXXXX XXXXXXXX		PCNH10 [R/W] 0000000 -	PCNL10 [R/W] 000000 - 0	
000168_H	PTMR11 [R] 11111111 11111111		PCSR11 [W] XXXXXXXX XXXXXXXX		PPG 11

Address	Register				Block
	+0	+1	+2	+3	
00016C$_H$	PDUT11 [W] XXXXXXXX XXXXXXXX		PCNH11 [R/W] 0000000 -	PCNL11 [R/W] 000000 - 0	
000170$_H$	~~P0TMCSRH [R/W] -0000000~~	~~P0TMCSRL [R/W] 01000000~~	~~P1TMCSRH [R/W] -0000000~~	~~P1TMCSRL [R/W] 01000000~~	~~Pulse Frequency Modulator~~
000174$_H$	~~P0TMRLR [W] XXXXXXXX XXXXXXXX~~		~~P0TMR [R] XXXXXXXX XXXXXXXX~~		
000178$_H$	~~P1TMRLR [W] XXXXXXXX XXXXXXXX~~		~~P1TMR [R] XXXXXXXX XXXXXXXX~~		
00017C$_H$	reserved				
000180$_H$	res.	ICS01 [R/W] 00000000	res.	ICS23 [R/W] 00000000	Input Capture 0-3
000184$_H$	IPCP0 [R] XXXXXXXX XXXXXXXX		IPCP1 [R] XXXXXXXX XXXXXXXX		
000188$_H$	IPCP2 [R] XXXXXXXX XXXXXXXX		IPCP3 [R] XXXXXXXX XXXXXXXX		
00018C$_H$	OCS01 [R/W] - - - 0 - - 00 0000 - - 00		OCS23 [R/W] - - - 0 - - 00 0000 - - 00		Output Compare 0-3
000190$_H$	OCCP0 [R/W] XXXXXXXX XXXXXXXX		OCCP1 [R/W] XXXXXXXX XXXXXXXX		
000194$_H$	OCCP2 [R/W] XXXXXXXX XXXXXXXX		OCCP3 [R/W] XXXXXXXX XXXXXXXX		

Address	Register				Block
	+0	+1	+2	+3	
000198_H	SGCRH [R/W] 0000 - - 00	SGCRL [R/W] - - 0 - - 000	SGFR [R/W, R] XXXXXXXX XXXXXXXX		Sound Generator
$00019C_H$	SGAR [R/W] 00000000	res.	SGTR [R/W] XXXXXXXX	SGDR [R/W] XXXXXXXX	
$0001A0_H$	ADERH [R/W] 00000000 00000000		ADERL [R/W] 00000000 00000000		A/D Converter
0001A4	ADCS1 [R/W] 00000000	ADCS0 [R/W] 00000000	ADCR1 [R] 000000XX	ADCR0 [R] XXXXXXXX	
$0001A8_H$	ADCT1 [R/W] 00010000	ADCT0 [R/W] 00101100	ADSCH [R/W] - - - 00000	ADECH [R/W] - - - 00000	
$0001AC_H$	res.	ACSR0 [R/W] -11XXX00	res.	~~ACSR1 [R/W] -11XXX00~~	Alarm Comparator 0-1
$0001B0_H$	TMRLR0 [W] XXXXXXXX XXXXXXXX		TMR0 [R] XXXXXXXX XXXXXXXX		Reload Timer 0 (PPG 0-1)
$0001B4_H$	reserved		TMCSRH0 [R/W] - - - 00000	TMCSRL0 [R/W] 0 - 000000	
$0001B8_H$	TMRLR1 [W] XXXXXXXX XXXXXXXX		TMR1 [R] XXXXXXXX XXXXXXXX		Reload Timer 1 (PPG 2-3)
$0001BC_H$	reserved		TMCSRH1 [R/W] - - - 00000	TMCSRL1 [R/W] 0 - 000000	
$0001C0_H$	TMRLR2 [W] XXXXXXXX XXXXXXXX		TMR2 [R] XXXXXXXX XXXXXXXX		Reload Timer 2 (PPG 4-5)

Address	Register				Block
	+0	+1	+2	+3	
$0001C4_H$	reserved		TMCSRH2 [R/W] - - - 00000	TMCSRL2 [R/W] 0 - 000000	
$0001C8_H$	TMRLR3 [W] XXXXXXXX XXXXXXXX		TMR3 [R] XXXXXXXX XXXXXXXX		Reload Timer 3 (PPG 6-7)
$0001CC_H$	reserved		TMCSRH3 [R/W] - - - 00000	TMCSRL3 [R/W] 0 - 000000	
$0001D0_H$	TMRLR4 [W] XXXXXXXX XXXXXXXX		TMR4 [R] XXXXXXXX XXXXXXXX		Reload Timer 4 (PPG 8-9)
$0001D4_H$	reserved		TMCSRH4 [R/W] - - - 00000	TMCSRL4 [R/W] 0 - 000000	
$0001D8_H$	TMRLR5 [W] XXXXXXXX XXXXXXXX		TMR5 [R] XXXXXXXX XXXXXXXX		Reload Timer 5 (PPG 10-11)
$0001DC_H$	reserved		TMCSRH5 [R/W] - - - 00000	TMCSRL5 [R/W] 0 - 000000	
$0001E0_H$	TMRLR6 [W] XXXXXXXX XXXXXXXX		TMR6 [R] XXXXXXXX XXXXXXXX		Reload Timer 6 (PPG 12-13)
$0001E4_H$	reserved		TMCSRH6 [R/W] - - - 00000	TMCSRL6 [R/W] 0 - 000000	
$0001E8_H$	TMRLR7 [W] XXXXXXXX XXXXXXXX		TMR7 [R] XXXXXXXX XXXXXXXX		Reload Timer 7 (PPG 14-15) (ADC)
$0001EC_H$	reserved		TMCSRH7 [R/W] - - - 00000	TMCSRL7 [R/W] 0 - 000000	

Address	Register				Block
	+0	+1	+2	+3	
$0001F0_H$	TCDT0 [R/W] XXXXXXXX XXXXXXXX		res.	TCCS0 [R/W] 00000000	Free Running Timer 0 (ICU 0-1)
$0001F4_H$	TCDT1 [R/W] XXXXXXXX XXXXXXXX		res.	TCCS1 [R/W] 00000000	Free Running Timer 1 (ICU 2-3)
$0001F8_H$	TCDT2 [R/W] XXXXXXXX XXXXXXXX		res.	TCCS2 [R/W] 00000000	Free Running Timer 2 (OCU 0-1)
$0001FC_H$	TCDT3 [R/W] XXXXXXXX XXXXXXXX		res.	TCCS3 [R/W] 00000000	Free Running Timer 3 (OCU 2-3)
000200_H	DMACA0 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
000204_H	DMACB0 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000208_H	DMACA1 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
$00020C_H$	DMACB1 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000210_H	DMACA2 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000214_H	DMACB2 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000218_H	DMACA3 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				

Address	Register				Block
	+0	+1	+2	+3	
$00021C_H$	DMACB3 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000220_H	DMACA4 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000224_H	DMACB4 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000228_H - $00023C_H$	reserved				
000240_H	DMACR [R/W] 00 - - 0000	reserved			
000244_H - $00024C_H$	reserved				
000250_H	DMATEST0 [R/W] XXXXXXXX 00000000 00000000 0000XXXX				DMA Test (do not use)
000254_H	DMATEST1 [R] XXXXXXXX XXXXX000 00000000 00000000				
000258_H - $0002CC_H$	reserved				
$0002D0_H$	res.	ICS045 [R/W] 00000000	res.	ICS67 [R/W] 00000000	Input Capture 4-7
$0002D4_H$	IPCP4 [R] XXXXXXXX XXXXXXXX		IPCP5 [R] XXXXXXXX XXXXXXXX		

Address	Register				Block
	+0	+1	+2	+3	
0002D8$_H$	IPCP6 [R] XXXXXXXX XXXXXXXX		IPCP7 [R] XXXXXXXX XXXXXXXX		
0002DC$_H$	OCS45 [R/W] - - - 0 - - 00 0000 - - 00		OCS67 [R/W] - - - 0 - - 00 0000 - - 00		Output Compare 4-7
0002E0$_H$	OCCP4 [R/W] XXXXXXXX XXXXXXXX		OCCP5 [R/W] XXXXXXXX XXXXXXXX		
0002E4$_H$	OCCP6 [R/W] XXXXXXXX XXXXXXXX		OCCP7 [R/W] XXXXXXXX XXXXXXXX		
0002E8$_H$ - 0002EC$_H$	reserved				
0002F0$_H$	TCDT4 [R/W] XXXXXXXX XXXXXXXX		res.	TCCS4 [R/W] 00000000	Free Running Timer 4 (ICU 4-5)
0002F4$_H$	TCDT5 [R/W] XXXXXXXX XXXXXXXX		res.	TCCS5 [R/W] 00000000	Free Running Timer 5 (ICU 6-7)
0002F8$_H$	TCDT6 [R/W] XXXXXXXX XXXXXXXX		res.	TCCS6 [R/W] 00000000	Free Running Timer 6 (OCU 4-5)
0002FC$_H$	TCDT7 [R/W] XXXXXXXX XXXXXXXX		res.	TCCS7 [R/W] 00000000	Free Running Timer 7 (OCU 6-7)
000300$_H$	UDRC1 [W] 00000000	UDRC0 [W] 00000000	UDCR1 [R] 00000000	UDCR0 [R] 00000000	Up/Down Counter 0-1
000304$_H$	UDCCH0 [R/W] 00000000	UDCCL0 [R/W] 00001000	res.	UDCS0 [R/W] 00000000	

Address	Register				Block
	+0	+1	+2	+3	
000308$_H$	UDCCH1 [R/W] 00000000	UDCCL1 [R/W] 00001000	res.	UDCS1 [R/W] 00000000	
00030C$_H$	reserved				
000310$_H$	~~UDRC3 [W] 00000000~~	~~UDRC2 [W] 00000000~~	~~UDCR3 [R] 00000000~~	~~UDCR2 [R] 00000000~~	~~Up/Down Counter 2-3~~
000314$_H$	~~UDCCH2 [R/W] 00000000~~	~~UDCCL2 [R/W] 00001000~~	res.	~~UDCS2 [R/W] 00000000~~	
000318$_H$	~~UDCCH3 [R/W] 00000000~~	~~UDCCL3 [R/W] 00001000~~	res.	~~UDCS3 [R/W] 00000000~~	
00031C$_H$	reserved				
000320$_H$	GCN13 [R/W] 00110010 00010000		res.	GCN23 [R/W] - - - - 0000	PPG Control 12-15
000324$_H$ - 00032C$_H$	reserved				
000330$_H$	PTMR12 [R] 11111111 11111111		PCSR12 [W] XXXXXXXX XXXXXXXX		PPG 12
000334$_H$	PDUT12 [W] XXXXXXXX XXXXXXXX		PCNH12 [R/W] 0000000 -	PCNL12 [R/W] 000000 - 0	
000338$_H$	PTMR13 [R] 11111111 11111111		PCSR13 [W] XXXXXXXX XXXXXXXX		PPG 13

Address	Register				Block
	+0	+1	+2	+3	
00033C$_H$	PDUT13 [W] XXXXXXXX XXXXXXXX		PCNH13 [R/W] 0000000 -	PCNL13 [R/W] 000000 - 0	
000340$_H$	PTMR14 [R] 11111111 11111111		PCSR14 [W] XXXXXXXX XXXXXXXX		PPG 14
000344$_H$	PDUT14 [W] XXXXXXXX XXXXXXXX		PCNH14 [R/W] 0000000 -	PCNL14 [R/W] 000000 - 0	
000348$_H$	PTMR15 [R] 11111111 11111111		PCSR15 [W] XXXXXXXX XXXXXXXX		PPG 15
00034C$_H$	PDUT15 [W] XXXXXXXX XXXXXXXX		PCNH15 [R/W] 0000000 -	PCNL15 [R/W] 000000 - 0	
000350$_H$ - 00035C$_H$	reserved				
000360$_H$	res.	~~DACR [R/W] ---000~~	res.	res.	~~D/A Converter~~
000364$_H$	~~DADR0 [R/W] XX XXXXXXXX~~		~~DADR1 [R/W] XX XXXXXXXX~~		
000368$_H$	~~IBCR2 [R/W] 00000000~~	~~IBSR2 [R] 00000000~~	~~ITBAH2 [R/W] ------00~~	~~ITBAL2 [R/W] 00000000~~	~~I2C 2~~
00036C$_H$	~~ITMKH2 [R/W] 00------11~~	~~ITMKL2 [R/W] 11111111~~	~~ISMK2 [R/W] 01111111~~	~~ISBA2 [R/W] -0000000~~	
000370$_H$	res.	~~IDAR2 [R/W] 00000000~~	~~ICCR2 [R/W] -0011111~~	res.	

Address	Register				Block
	+0	+1	+2	+3	
000374H	~~IBCR3 [R/W] 00000000~~	~~IBSR3 [R] 00000000~~	~~ITBAH3 [R/W] ------00~~	~~ITBAL3 [R/W] 00000000~~	~~I2C 3~~
000378$_H$	~~ITMKH3 [R/W] 00------11~~	~~ITMKL3 [R/W] 11111111~~	~~ISMK3 [R/W] 01111111~~	~~ISBA3 [R/W] -0000000~~	
00037C$_H$	res.	~~IDAR3 [R/W] 00000000~~	~~ICCR3 [R/W] -0011111~~	res.	
000380$_H$ - 00038C$_H$	reserved				
000390$_H$	ROMS ***[R]*** ***11111111 00000000***		res.		ROM Select Register
000394$_H$ - 0003BC$_H$	reserved				(do not use)
0003C0$_H$	reserved				~~I-Cache~~
0003C4$_H$	reserved			~~ISIZE [R/W] ------11~~	
0003D8$_H$ - 0003E0$_H$	reserved				
0003E4$_H$	reserved			~~ICHCR [R/W] 0-000000~~	~~I-Cache~~
0003E8$_H$ - 0003EC$_H$	reserved				(do not use)
0003F0$_H$	BSD0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Bit Search Module

Address	Register				Block
	+0	+1	+2	+3	
$0003F4_H$	BSD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0003F8_H$	BSDC [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0003FC_H$	BSRR [R] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000400_H - $00043C_H$	reserved				
000440_H	ICR00 [R/W] ---11111	ICR01 [R/W] ---11111	ICR02 [R/W] ---11111	ICR03 [R/W] ---11111	Interrupt Control Unit
000444_H	ICR04 [R/W] ---11111	ICR05 [R/W] ---11111	ICR06 [R/W] ---11111	ICR07 [R/W] ---11111	
000448_H	ICR08 [R/W] ---11111	ICR09 [R/W] ---11111	ICR10 [R/W] ---11111	ICR11 [R/W] ---11111	
$00044C_H$	ICR12 [R/W] ---11111	ICR13 [R/W] ---11111	ICR14 [R/W] ---11111	ICR15 [R/W] ---11111	
000450_H	ICR16 [R/W] ---11111	ICR17 [R/W] ---11111	ICR18 [R/W] ---11111	ICR19 [R/W] ---11111	
000454_H	***ICR20 [R/W] ---11111***	ICR21 [R/W] ---11111	ICR22 [R/W] ---11111	ICR23 [R/W] ---11111	
000458_H	ICR24 [R/W] ---11111	ICR25 [R/W] ---11111	ICR26 [R/W] ---11111	ICR27 [R/W] ---11111	

Address	Register				Block
	+0	+1	+2	+3	
$00045C_H$	ICR28 [R/W] ---11111	ICR29 [R/W] ---11111	***ICR30 [R/W] ---11111***	***ICR31 [R/W] ---11111***	
000460_H	***ICR32 [R/W] ---11111***	***ICR33 [R/W] ---11111***	***ICR34[R/W] ---11111***	***ICR35 [R/W] ---11111***	
000464_H	***ICR36 [R/W] ---11111***	***ICR37 [R/W] ---11111***	ICR38 [R/W] ---11111	ICR39 [R/W] ---11111	
000468_H	ICR40 [R/W] ---11111	ICR41 [R/W] ---11111	ICR42 [R/W] ---11111	ICR43 [R/W] ---11111	
$00046C_H$	ICR44 [R/W] ---11111	ICR45 [R/W] ---11111	ICR46 [R/W] ---11111	ICR47 [R/W] ---11111	
000470_H	ICR48 [R/W] ---11111	ICR49 [R/W] ---11111	ICR50 [R/W] ---11111	ICR51 [R/W] ---11111	
000474_H	ICR52 [R/W] ---11111	ICR53 [R/W] ---11111	ICR54 [R/W] ---11111	ICR55 [R/W] ---11111	
000478_H	ICR56 [R/W] ---11111	***ICR57 [R/W] ---11111***	ICR58 [R/W] ---11111	ICR59 [R/W] ---11111	
$00047C_H$	ICR60 [R/W] ---11111	ICR61 [R/W] ---11111	ICR62 [R/W] ---11111	ICR63 [R/W] ---11111	
000480_H	RSRR [R/W] 10000000	STCR [R/W] 00110011	TBCR [R/W] 00XXXX00	CTBR [W] XXXXXXXX	Clock Control Unit
000484_H	CLKR [R/W] - - - - 0000	WPR [W] XXXXXXXX	DIVR0 [R/W] 00000011	DIVR1 [R/W] 00000000	

Address	Register				Block
	+0	+1	+2	+3	
000488_H	~~CTEST [R/W] XXXX00XX~~	res.	res.	res.	~~C Unit Test~~ (do not use)
$00048C_H$	PLLDIVM [R/W] - - - - 0000	PLLDIVN [R/W] - - 000000	PLLDIVG [R/W] - - - - 0000	PLLMULG [R/W] 00000000	PLL Clock Gear Unit
000490_H	PLLCTRL [R/W] - - - - 0000	res.	res.	res.	
000494_H	OSCC1 [R/W] - - - - - 010	OSCS1 [R/W] 00001111	OSCC2 [R/W] - - - - - 010	OSCS2 [R/W] 00001111	Main/Sub Oscillator Control (do not use)
000498_H	PORTEN [R/W] - - - - - - 00	res.	res.	res.	Port Input Enable Control
$0004A0_H$	res.	WTCER [R/W] - - - - - - 00	WTCR [R/W] 00000000 000 - 00 - 0		Real Time Clock (Watch Timer)
$0004A4_H$	res.	WTBR [R/W] - - - XXXXX XXXXXXXX XXXXXXXX			
$0004A8_H$	WTHR [R/W] - - - 00000	WTMR [R/W] - - 000000	WTSR [R/W] - - 000000	res.	
$0004AC_H$	CSVTR [R/W] ***- - - 00010***	CSVCR [R/W] **-** 011100	CSCFG [R/W] 0X000000	CMCFG [R/W] 00000000	Clock-Supervisor / Selector / Monitor
$0004B0_H$	CUCR [R/W] - - - - - - - - - - - - 0 - - 00		CUTD [R/W] 10000000 00000000		Calibration Unit of Sub Oscillation
$0004B4_H$	CUTR1 [R] - - - - - - - - 00000000		CUTR2 [R] 00000000 00000000		

Address	Register				Block
	+0	+1	+2	+3	
0004B8$_H$	CMPR [R/W] - - 000010 11111101		res.	CMCR [R/W] - 001 - - 00	Clock Modulation
0004BC$_H$	CMT1 [R/W] 00000000 1 - - - 0000		CMT2 [R/W] - - 000000 - - 000000		
0004C0$_H$	CANPRE [R/W] 0 - - - 0000	~~CANCKD [R/W] - - 000000~~	res.	res.	CAN Clock Control
0004C4$_H$	LVSEL [R/W] 00000101	LVDET [R/W] 00000 - 00	HWWDE [R/W] - - - - - - 00	HWWD [R/W,W] 00011000	LV Detection / Hardware-Watchdog
0004C8$_H$	OSCRH [R/W] 000 - - 001	OSCRL [R/W] - - - - - 000	WPCRH [R/W] 000 - - 001	WPCRL [R/W] - - - - - - 00	Main-/Sub-Oscillation Stabilisation Timer
0004CC$_H$	OSCCR [R/W] - - - - - - 00	res.	REGSEL [R/W] - - 000100	REGCTR [R/W] - - - 0 - - 00	Main-Oscillation Standby Control / Main/Sub Regulator Control
0004D0$_H$	~~C340R [R/W] - - - - - - - 0~~	res.	~~EISSRH [R/W] 00000000~~	~~EISSRL [R/W] 00000000~~	~~340 Compatibility Mode~~ (do not use)
0004D4$_H$	~~SHDE [R/W] 0 - - - - - - -~~	res.	~~EXTE [R/W] 00000000~~	~~EXTF [R/W] 00000000~~	~~Supply Shut Down Mode~~ (do not use)
0004D8$_H$	~~EXTLV [R/W] 00000000 00000000~~		res.	res.	
0004DC$_H$ - 00063C$_H$	reserved				(do not use)

Address	Register				Block
	+0	+1	+2	+3	
000640_H	ASR0 [R/W] 00000000 00000000		ACR0 [R/W] 1111**00 00000000		* note at the end of the section
000644_H	ASR1 [R/W] XXXXXXXX XXXXXXXX		ACR1 [R/W] XXXXXXXX XXXXXXXX		
000648_H	ASR2 [R/W] XXXXXXXX XXXXXXXX		ACR2 [R/W] XXXXXXXX XXXXXXXX		External Bus Unit
$00064C_H$	ASR3 [R/W] XXXXXXXX XXXXXXXX		ACR3 [R/W] XXXXXXXX XXXXXXXX		
000650_H	ASR4 [R/W] XXXXXXXX XXXXXXXX		ACR4 [R/W] XXXXXXXX XXXXXXXX		
000654_H	ASR5 [R/W] XXXXXXXX XXXXXXXX		ACR5 [R/W] XXXXXXXX XXXXXXXX		
000658_H	ASR6 [R/W] XXXXXXXX XXXXXXXX		ACR6 [R/W] XXXXXXXX XXXXXXXX		
$00065C_H$	ASR7 [R/W] XXXXXXXX XXXXXXXX		ACR7 [R/W] XXXXXXXX XXXXXXXX		
000660_H	AWR0 [R/W] 01111111 11111*11		AWR1 [R/W] XXXXXXXX XXXXXXXX		
000664_H	AWR2 [R/W] XXXXXXXX XXXXXXXX		AWR3 [R/W] XXXXXXXX XXXXXXXX		
000668_H	AWR4 [R/W] XXXXXXXX XXXXXXXX		AWR5 [R/W] XXXXXXXX XXXXXXXX		

Address	Register				Block
	+0	+1	+2	+3	
00066C$_H$	AWR6 [R/W] XXXXXXXX XXXXXXXX		AWR7 [R/W] XXXXXXXX XXXXXXXX		
000670$_H$	MCRA [R/W] XXXXXXXX	MCRB [R/W] XXXXXXXX	reserved		
000674$_H$	reserved				
000678$_H$	IOWR0 [R/W] XXXXXXXX	IOWR1 [R/W] XXXXXXXX	IOWR2 [R/W] XXXXXXXX	IOWR3 [R/W] XXXXXXXX	
00067C$_H$	reserved				
000680$_H$	CSER [R/W] 00000001	CHER [R/W] 11111111	res.	TCR [R/W] 0000****	
000684$_H$	RCRH [R/W] 00XXXXXX	RCRL [R/W] XXXX0XXX	reserved		
000688$_H$ - 0007F8$_H$	reserved				
ACR0[11:10] depends on Modevector fetch information on buswidth TCR[3:0] INIT value = 0000, keeps value after RST					
0007FC$_H$	res.	MODR [W] XXXXXXXX	res.	res.	Mode Register
000800$_H$ - 000BFC$_H$	reserved				DSU4 / RTM
000C00$_H$	~~TVCTW [W] XXXXXXXX~~	~~TVCTR [R] XXXXXXX~~	res.	~~IOS [R/W] 00000000~~	~~I Unit Test~~ (do not use)

Address	Register				Block
	+0	+1	+2	+3	
$000C04_H$ - $000CFC_H$	reserved				(do not use)
$000D00_H$	PDRD00 [R] XXXXXXXX	PDRD01 [R] XXXXXXXX	~~PDRD02 [R] XXXXXXXX~~	~~PDRD03 [R] XXXXXXXX~~	R-bus Port Data Direct Read Register
$000D04_H$	~~PDRD04 [R] XXXXXXXX~~	PDRD05 [R] ***- - XXXXXX***	PDRD06 [R] XXXXXXXX	PDRD07 [R] XXXXXXXX	
$000D08_H$	PDRD08 [R] ***X - - X - - -X***	PDRD09 [R] ***- - - - - - XX***	PDRD10 [R] ***- - - - - - - X***	~~PDRD11 [R] XXXXXXXX~~	
$000D0C_H$	~~PDRD12 [R] XXXXXXXX~~	~~PDRD13 [R] XXXXXXXX~~	PDRD14 [R] XXXXXXXX	PDRD15 [R] XXXXXXXX	
$000D10_H$	PDRD16 [R] XXXXXXXX	PDRD17 [R] XXXXXXXX	PDRD18 [R] ***- XXX - XXX***	PDRD19 [R] ***- XXX - XXX***	
$000D14_H$	PDRD20 [R] ***- XXX - XXX***	PDRD21 [R] ***- - - - - - - X***	PDRD22 [R] XXXXXXXX	PDRD23 [R] XXXXXXXX	
$000D18_H$	PDRD24 [R] XXXXXXXX	~~PDRD25 [R] XXXXXXXX~~	PDRD26 [R] XXXXXXXX	PDRD27 [R] XXXXXXXX	
$000D1C_H$	PDRD28 [R] XXXXXXXX	PDRD29 [R] XXXXXXXX	~~PDRD30 [R] XXXXXXXX~~	~~PDRD31 [R] XXXXXXXX~~	
$000D20_H$	~~PDRD32 [R] XXXXXXXX~~	~~PDRD33 [R] XXXXXXXX~~	~~PDRD34 [R] XXXXXXXX~~	~~PDRD35 [R] XXXXXXXX~~	
$000D24_H$ - $000D3C_H$	reserved				(do not use)

Address	Register				Block
	+0	+1	+2	+3	
$000D40_H$	DDR00 [R/W] 00000000	DDR01 [R/W] 00000000	~~DDR02 [R/W]~~ ~~00000000~~	~~DDR03 [R/W]~~ ~~00000000~~	R-bus Port Direction Register
$000D44_H$	~~DDR04 [R/W]~~ ~~00000000~~	DDR05 [R/W] ***- - 000000***	DDR06 [R/W] 00000000	DDR07 [R/W] 00000000	
$000D48_H$	DDR08 [R/W] ***0 - - 0 - - -0***	DDR09 [R/W] ***- - - - - - 00***	DDR10 [R/W] ***- - - - - - -0***	~~DDR11 [R/W]~~ ~~00000000~~	
$000D4C_H$	~~DDR12 [R/W]~~ ~~00000000~~	~~DDR13 [R/W]~~ ~~00000000~~	DDR14 [R/W] 00000000	DDR15 [R/W] 00000000	
$000D50_H$	DDR16 [R/W] 00000000	DDR17 [R/W] 00000000	DDR18 [R/W] ***- 000 - 000***	DDR19 [R/W] ***- 000 - 000***	
$000D54_H$	DDR20 [R/W] ***- 000 - 000***	DDR21 [R/W] ***- - - - - - 00***	DDR22 [R/W] 00000000	DDR23 [R/W] 00000000	
$000D58_H$	DDR24 [R/W] 00000000	~~DDR25 [R/W]~~ ~~00000000~~	DDR26 [R/W] 00000000	DDR27 [R/W] 00000000	
$000D5C_H$	DDR28 [R/W] 00000000	DDR29 [R/W] 00000000	~~DDR30 [R/W]~~ ~~00000000~~	~~DDR31 [R/W]~~ ~~00000000~~	
$000D60_H$	~~DDR32 [R/W]~~ ~~00000000~~	~~DDR33 [R/W]~~ ~~00000000~~	~~DDR34 [R/W]~~ ~~00000000~~	~~DDR35 [R/W]~~ ~~00000000~~	
$000D64_H$ - $000D7C_H$	reserved				(do not use)
$000D80_H$	PFR00 [R/W] 11111111	PFR01 [R/W] 11111111	~~PFR02 [R/W]~~ ~~11111111~~	~~PFR03 [R/W]~~ ~~11111111~~	R-bus Port Function Register

Address	Register				Block
	+0	+1	+2	+3	
000D84H	~~PFR04 [R/W] 11111111~~	PFR05 [R/W] ***- - 111111***	PFR06 [R/W] 11111111	PFR07 [R/W] 11111111	
000D88H	PFR08 [R/W] ***1 - - 1 - - - 1***	PFR09 [R/W] ***- - - - - - 11***	PFR10 [R/W] ***- - - - - - - -1***	~~PFR11 [R/W] 00000000~~	
000D8CH	~~PFR12 [R/W] 00000000~~	~~PFR13 [R/W] 00000000~~	PFR14 [R/W] 00000000	PFR15 [R/W] 00000000	
000D90H	PFR16 [R/W] 00000000	PFR17 [R/W] 00000000	PFR18 [R/W] ***- 000 - 000***	PFR19 [R/W] ***- 000 - 000***	
000D94H	PFR20 [R/W] ***- 000 - 000***	PFR21 [R/W] ***- - - - - - 00***	PFR22 [R/W] 00000000	PFR23 [R/W] 00000000	
000D98H	PFR24 [R/W] 00000000	~~PFR25 [R/W] 00000000~~	PFR26 [R/W] 00000000	PFR27 [R/W] 00000000	
000D9CH	PFR28 [R/W] 00000000	PFR29 [R/W] 00000000	~~PFR30 [R/W] 00000000~~	~~PFR31 [R/W] 00000000~~	
000DA0H	~~PFR32 [R/W] 00000000~~	~~PFR33 [R/W] 00000000~~	~~PFR34 [R/W] 00000000~~	~~PFR35 [R/W] 00000000~~	
000DA4H - 000DBCH	reserved				
000DC0H	~~EPFR00 [R/W] 00000000~~	~~EPFR01 [R/W] 00000000~~	~~EPFR02 [R/W] 00000000~~	~~EPFR03 [R/W] 00000000~~	R-bus Port Extra Function Register
000DC4H	~~EPFR04 [R/W] 00000000~~	~~EPFR05 [R/W] 00000000~~	~~EPFR06 [R/W] 00000000~~	~~EPFR07 [R/W] 00000000~~	

Address	Register				Block
	+0	+1	+2	+3	
000DC8$_H$	~~EPFR08 [R/W] 00000000~~	~~EPFR09 [R/W] 00000000~~	EPFR10 [R/W] ***- - - - - - - 0***	~~EPFR11 [R/W] 00000000~~	
000DCC$_H$	~~EPFR12 [R/W] 00000000~~	~~EPFR13 [R/W] 00000000~~	EPFR14 [R/W] 00000000	EPFR15 [R/W] 00000000	
000DD0$_H$	EPFR16 [R/W] ***0 - 00 - - - -***	~~EPFR17 [R/W] 00000000~~	EPFR18 [R/W] ***- 000 - 000***	EPFR19 [R/W] ***- 000 - 000***	
000DD4$_H$	EPFR20 [R/W] ***- 000 - 000***	EPFR21 [R/W] ***- - - - - - 00***	~~EPFR22 [R/W] 00000000~~	~~EPFR23 [R/W] 00000000~~	
000DD8$_H$	~~EPFR24 [R/W] 00000000~~	~~EPFR25 [R/W] 00000000~~	EPFR26 [R/W] 00000000	EPFR27 [R/W] 00000000	
000DDC$_H$	~~EPFR28 [R/W] 00000000~~	~~EPFR29 [R/W] 00000000~~	~~EPFR30 [R/W] 00000000~~	~~EPFR31 [R/W] 00000000~~	
000DE0$_H$	~~EPFR32 [R/W] 00000000~~	~~EPFR33 [R/W] 00000000~~	~~EPFR34 [R/W] 00000000~~	~~EPFR35 [R/W] 00000000~~	
000DE4$_H$ - 000DFC$_H$	reserved				(do not use)
000E00$_H$	PODR00 [R/W] 00000000	PODR01 [R/W] 00000000	~~PODR02 [R/W] 00000000~~	~~PODR03 [R/W] 00000000~~	R-bus Port Output Drive Select Register
000E04$_H$	~~PODR04 [R/W] 00000000~~	PODR05 [R/W] ***- - 000000***	PODR06 [R/W] 00000000	PODR07 [R/W] 00000000	
000E08$_H$	PODR08 [R/W] ***0 - - 0 - - - 0***	PODR09 [R/W] ***- - - - - - 00***	PODR10 [R/W] ***- - - - - - - 0***	~~PODR11 [R/W] 00000000~~	

Address	Register				Block
	+0	+1	+2	+3	
000E0C$_H$	~~PODR12 [R/W] 00000000~~	~~PODR13 [R/W] 00000000~~	PODR14 [R/W] 00000000	PODR15 [R/W] 00000000	
000E10$_H$	PODR16 [R/W] 00000000	PODR17 [R/W] 00000000	PODR18 [R/W] ***- 000 - 000***	PODR19 [R/W] ***- 000 - 000***	
000E14$_H$	PODR20 [R/W] ***- 000 - 000***	PODR21 [R/W] ***- - - - - - 00***	PODR22 [R/W] 00000000	PODR23 [R/W] 00000000	
000E18$_H$	PODR24 [R/W] 00000000	~~PODR25 [R/W] 00000000~~	PODR26 [R/W] 00000000	PODR27 [R/W] 00000000	
000E1C$_H$	PODR28 [R/W] 00000000	PODR29 [R/W] 00000000	~~PODR30 [R/W] 00000000~~	~~PODR31 [R/W] 00000000~~	
000E20$_H$	~~PODR32 [R/W] 00000000~~	~~PODR33 [R/W] 00000000~~	~~PODR34 [R/W] 00000000~~	~~PODR35 [R/W] 00000000~~	
000E24$_H$ - 000E3C$_H$	reserved				
000E40$_H$	PILR00 [R/W] 00000000	PILR01 [R/W] 00000000	~~PILR02 [R/W] 00000000~~	~~PILR03 [R/W] 00000000~~	R-bus Port Input Level Select Register
000E44$_H$	~~PILR04 [R/W] 00000000~~	PILR05 [R/W] ***- - 000000***	PILR06 [R/W] 00000000	PILR07 [R/W] 00000000	
000E48$_H$	PILR08 [R/W] ***0 - - 0 - - - 0***	PILR09 [R/W] ***- - - - - - 00***	PILR10 [R/W] ***- - - - - - - 0***	~~PILR11 [R/W] 00000000~~	
000E4C$_H$	~~PILR12 [R/W] 00000000~~	~~PILR13 [R/W] 00000000~~	PILR14 [R/W] 00000000	PILR15 [R/W] 00000000	

Address	Register				Block
	+0	+1	+2	+3	
$000E50_H$	PILR16 [R/W] 00000000	PILR17 [R/W] 00000000	PILR18 [R/W] ***- - - - - 000***	PILR19 [R/W] ***- 000 - 000***	
$000E54_H$	PILR20 [R/W] ***- 000 - 000***	PILR21 [R/W] ***- - - - - - 00***	PILR22 [R/W] 00000000	PILR23 [R/W] 00000000	
$000E58_H$	PILR24 [R/W] 00000000	~~PILR25 [R/W]~~ ~~00000000~~	PILR26 [R/W] 00000000	PILR27 [R/W] 00000000	
$000E5C_H$	PILR28 [R/W] 00000000	PILR29 [R/W] 00000000	~~PILR30 [R/W]~~ ~~00000000~~	~~PILR31 [R/W]~~ ~~00000000~~	
$000E60_H$	~~PILR32 [R/W]~~ ~~00000000~~	~~PILR33 [R/W]~~ ~~00000000~~	~~PILR34 [R/W]~~ ~~00000000~~	~~PILR35 [R/W]~~ ~~00000000~~	
$000E64_H$ - $000E7C_H$	reserved				(do not use)
$000E80_H$	EPILR00 [R/W] 00000000	EPILR01 [R/W] 00000000	~~EPILR02 [R/W]~~ ~~00000000~~	~~EPILR03 [R/W]~~ ~~00000000~~	R-bus Port Extra Input Level Select Register
$000E84_H$	~~EPILR04 [R/W]~~ ~~00000000~~	EPILR05 [R/W] ***- - 000000***	EPILR06 [R/W] 00000000	EPILR07 [R/W] 00000000	
$000E88_H$	EPILR08 [R/W] ***0 - - 0- - - 0***	EPILR09 [R/W] ***- - - - - - 00***	EPILR10 [R/W] ***- - - - - - - 0***	~~EPILR11 [R/W]~~ ~~00000000~~	
$000E8C_H$	~~EPILR12 [R/W]~~ ~~00000000~~	~~EPILR13 [R/W]~~ ~~00000000~~	EPILR14 [R/W] 00000000	EPILR15 [R/W] 00000000	
$000E90_H$	EPILR16 [R/W] 00000000	EPILR17 [R/W] 00000000	EPILR18 [R/W] ***- - - - - 000***	EPILR19 [R/W] ***- 000 - 000***	

Address	Register				Block
	+0	+1	+2	+3	
$000E94_H$	EPILR20 [R/W] ***- 000 - 000***	EPILR21 [R/W] ***- - - - - - 00***	EPILR22 [R/W] 00000000	EPILR23 [R/W] 00000000	
$000E98_H$	EPILR24 [R/W] 00000000	~~EPILR25 [R/W]~~ ~~00000000~~	EPILR26 [R/W] 00000000	EPILR27 [R/W] 00000000	
$000E9C_H$	EPILR28 [R/W] 00000000	EPILR29 [R/W] 00000000	~~EPILR30 [R/W]~~ ~~00000000~~	~~EPILR31 [R/W]~~ ~~00000000~~	
$000EA0_H$	~~EPILR32 [R/W]~~ ~~00000000~~	~~EPILR33 [R/W]~~ ~~00000000~~	~~EPILR34 [R/W]~~ ~~00000000~~	~~EPILR35 [R/W]~~ ~~00000000~~	
$000EA4_H$ - $000EBC_H$	reserved				(do not use)
$000EC0_H$	PPER00 [R/W] 00000000	PPER01 [R/W] 00000000	~~PPER02 [R/W]~~ ~~00000000~~	~~PPER03 [R/W]~~ ~~00000000~~	R-bus Port Pull-Up/Down Enable Register
$000EC4_H$	~~PPER04 [R/W]~~ ~~00000000~~	PPER05 [R/W] ***- - 000000***	PPER06 [R/W] 00000000	PPER07 [R/W] 00000000	
$000EC8_H$	PPER08 [R/W] ***0 - - 0 - - - 0***	PPER09 [R/W] ***- - - - - - 00***	PPER10 [R/W] ***- - - - - - - 0***	~~PPER11 [R/W]~~ ~~00000000~~	
$000ECC_H$	~~PPER12 [R/W]~~ ~~00000000~~	~~PPER13 [R/W]~~ ~~00000000~~	PPER14 [R/W] 00000000	PPER15 [R/W] 00000000	
$000ED0_H$	PPER16 [R/W] 00000000	PPER17 [R/W] 00000000	PPER18 [R/W] ***- 000 - 000***	PPER19 [R/W] ***- 000 - 000***	
$000ED4_H$	PPER20 [R/W] ***- 000 - 000***	PPER21 [R/W] ***- - - - - - 00***	PPER22 [R/W] 00000000	PPER23 [R/W] 00000000	

Address	Register				Block
	+0	+1	+2	+3	
000ED8$_H$	PPER24 [R/W] 00000000	~~PPER25 [R/W] 00000000~~	PPER26 [R/W] 00000000	PPER27 [R/W] 00000000	
000EDC$_H$	PPER28 [R/W] 00000000	PPER29 [R/W] 00000000	~~PPER30 [R/W] 00000000~~	~~PPER31 [R/W] 00000000~~	
000EE0$_H$	~~PPER32 [R/W] 00000000~~	~~PPER33 [R/W] 00000000~~	~~PPER34 [R/W] 00000000~~	~~PPER35 [R/W] 00000000~~	
000EE4$_H$ - 000EFC$_H$	reserved				
000F00$_H$	PPCR00 [R/W] 11111111	PPCR01 [R/W] 11111111	~~PPCR02 [R/W] 11111111~~	~~PPCR03 [R/W] 11111111~~	R-bus Port Pull-Up/Down Control Register
000F04$_H$	~~PPCR04 [R/W] 11111111~~	PPCR05 [R/W] ***- - 111111***	PPCR06 [R/W] 11111111	PPCR07 [R/W] 11111111	
000F08$_H$	PPCR08 [R/W] ***1 - - 1 - - - 1***	PPCR09 [R/W] ***- - - - - - 11***	PPCR10 [R/W] ***- - - - - - - 1***	~~PPCR11 [R/W] 11111111~~	
000F0C$_H$	~~PPCR12 [R/W] 11111111~~	~~PPCR13 [R/W] 11111111~~	PPCR14 [R/W] ***00000000***	PPCR15 [R/W] 11111111	
000F10$_H$	PPCR16 [R/W] ***00000000***	PPCR17 [R/W] ***00000000***	PPCR18 [R/W] ***- 111- 111***	PPCR19 [R/W] ***- 111- 111***	
000F14$_H$	PPCR20 [R/W] ***- 111- 111***	PPCR21 [R/W] ***- - - - - - 11***	PPCR22 [R/W] 11111111	PPCR23 [R/W] 11111111	
000F18$_H$	PPCR24 [R/W] 11111111	~~PPCR25 [R/W] 11111111~~	PPCR26 [R/W] 11111111	PPCR27 [R/W] 11111111	

Address	Register				Block
	+0	+1	+2	+3	
$000F1C_H$	PPCR28 [R/W] 11111111	PPCR29 [R/W] 11111111	~~PPCR30 [R/W] 11111111~~	~~PPCR31 [R/W] 11111111~~	
$000F20_H$	~~PPCR32 [R/W] 11111111~~	~~PPCR33 [R/W] 11111111~~	~~PPCR34 [R/W] 11111111~~	~~PPCR35 [R/W] 11111111~~	
$000F24_H$ - $000F3C_H$	reserved				(do not use)

Address	Register				Block
	+0	+1	+2	+3	
001000_H	DMASA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
001004_H	DMADA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001008_H	DMASA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00100C_H$	DMADA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001010_H	DMASA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001014_H	DMADA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001018_H	DMASA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00101C_H$	DMADA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001020_H	DMASA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001024_H	DMADA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001028_H - $003FFC_H$	reserved				(do not use)

Address	Register				Block
	+0	+1	+2	+3	
004000_H - $005FFC_H$	Instruction RAM(8kB)				Direct mapped cache
006000_H - $006FFC_H$	reserved				(do not use)
007000_H	FMCS [R/W] 01101000	FMCR [R/W] - - - - 0000	FCHCR [R/W] - - - - - - 00 10000011		Flash Memory/ I-Cache Control Register
007004_H	FMWT [R/W] 11111111 11111111		res.	FMPS [R/W] - - - - - 000	
007008_H	FMAC [R] 00000000 00000000 00000000 00000000				
$00700C_H$	~~FCHA0 [R/W] 000000 00000000 00000000~~				~~I-Cache Non-cacheable area setting Register~~
007010_H	~~FCHA1 [R/W] 000000 00000000 00000000~~				
007014_H - $007FFC_H$	reserved				
008000_H - $00BFFC_H$	MB91F467BA Boot-ROM size is 4kB : **$00B000_H$ - $00BFFC_H$** (instruction access is 1 waitcycle, data access is 1 waitcycle)				Boot ROM 4 kB
$00C000_H$	CTRLR0 [R/W] 00000000 00000001		STATR0 [R/W] 00000000 00000000		CAN 0 Control Register
$00C004_H$	ERRCNT0 [R] 00000000 00000000		BTR0 [R/W] 00100011 00000001		
$00C008_H$	INTR0 [R] 00000000 00000000		TESTR0 [R/W] 00000000 X0000000		

Address	Register				Block
	+0	+1	+2	+3	
$00C00C_H$	BRPE0 [R/W] 00000000 00000000		CBSYNC0 *2		
$00C010_H$	IF1CREQ0 [R/W] 00000000 00000001		IF1CMSK0 [R/W] 00000000 00000000		CAN 0 IF 1 Register
$00C014_H$	IF1MSK20 [R/W] 11111111 11111111		IF1MSK10 [R/W] 11111111 11111111		
$00C018_H$	IF1ARB20 [R/W] 00000000 00000000		IF1ARB10 [R/W] 00000000 00000000		
$00C01C_H$	IF1MCTR0 [R/W] 00000000 00000000		res.		
$00C020_H$	IF1DTA10 [R/W] 00000000 00000000		IF1DTA20 [R/W] 00000000 00000000		
$00C024_H$	IF1DTB10 [R/W] 00000000 00000000		IF1DTB20 [R/W] 00000000 00000000		
$00C028_H$ - $00C02C_H$	reserved				
$00C030_H$	*IF1DTA20 [R/W]* *00000000 00000000*		*IF1DTA10 [R/W]* *00000000 00000000*		
$00C034_H$	*IF1DTB20 [R/W]* *00000000 00000000*		*IF1DTB10 [R/W]* *00000000 00000000*		
$00C038_H$ - $00C03C_H$	reserved				

Address	Register				Block
	+0	+1	+2	+3	
$00C040_H$	IF2CREQ0 [R/W] 00000000 00000001		IF2CMSK0 [R/W] 00000000 00000000		CAN 0 IF 2 Register
$00C044_H$	IF2MSK20 [R/W] 11111111 11111111		IF2MSK10 [R/W] 11111111 11111111		
$00C048_H$	IF2ARB20 [R/W] 00000000 00000000		IF2ARB10 [R/W] 00000000 00000000		
$00C04C_H$	IF2MCTR0 [R/W] 00000000 00000000		res.		
$00C050_H$	IF2DTA10 [R/W] 00000000 00000000		IF2DTA20 [R/W] 00000000 00000000		
$00C054_H$	IF2DTB10 [R/W] 00000000 00000000		IF2DTB20 [R/W] 00000000 00000000		
$00C058_H$ - $00C05C_H$	reserved				
$00C060_H$	*IF2DTA20 [R/W]* *00000000 00000000*		*IF2DTA10 [R/W]* *00000000 00000000*		
$00C064_H$	*IF2DTB20 [R/W]* *00000000 00000000*		*IF2DTB10 [R/W]* *00000000 00000000*		
$00C068_H$ - $00C07C_H$	reserved				
$00C080_H$	TREQR20 [R] 00000000 00000000		TREQR10 [R] 00000000 00000000		CAN 0 Status Flags

Address	Register				Block
	+0	+1	+2	+3	
$00C084_H$	~~TREQR40 [R]~~ ~~00000000 00000000~~		~~TREQR30 [R]~~ ~~00000000 00000000~~		
$00C088_H$	~~TREQR60 [R]~~ ~~00000000 00000000~~		~~TREQR50 [R]~~ ~~00000000 00000000~~		
$00C08C_H$	~~TREQR80 [R]~~ ~~00000000 00000000~~		~~TREQR70 [R]~~ ~~00000000 00000000~~		
$00C090_H$	NEWDT20 [R] 00000000 00000000		NEWDT10 [R] 00000000 00000000		
$00C094_H$	~~NEWDT40 [R]~~ ~~00000000 00000000~~		~~NEWDT30 [R]~~ ~~00000000 00000000~~		
$00C098_H$	~~NEWDT60 [R]~~ ~~00000000 00000000~~		~~NEWDT50 [R]~~ ~~00000000 00000000~~		
$00C09C_H$	~~NEWDT80 [R]~~ ~~00000000 00000000~~		~~NEWDT70 [R]~~ ~~00000000 00000000~~		
$00C0A0_H$	INTPND20 [R] 00000000 00000000		INTPND10 [R] 00000000 00000000		
$00C0A4_H$	~~INTPND40 [R]~~ ~~00000000 00000000~~		~~INTPND30 [R]~~ ~~00000000 00000000~~		
$00C0A8_H$	~~INTPND60 [R]~~ ~~00000000 00000000~~		~~INTPND50 [R]~~ ~~00000000 00000000~~		
$00C0AC_H$	~~INTPND80 [R]~~ ~~00000000 00000000~~		~~INTPND70 [R]~~ ~~00000000 00000000~~		

Address	Register				Block
	+0	+1	+2	+3	
$00C0B0_H$	MSGVAL20 [R] 00000000 00000000		MSGVAL10 [R] 00000000 00000000		
$00C0B4_H$	~~MSGVAL40 [R]~~ ~~00000000 00000000~~		~~MSGVAL30 [R]~~ ~~00000000 00000000~~		
$00C0B8_H$	~~MSGVAL60 [R]~~ ~~00000000 00000000~~		~~MSGVAL50 [R]~~ ~~00000000 00000000~~		
$00C0BC_H$	~~MSGVAL80 [R]~~ ~~00000000 00000000~~		~~MSGVAL70 [R]~~ ~~00000000 00000000~~		
$00C0C0_H$ - $00C0FC_H$	reserved				
$00C100_H$	CTRLR1 [R/W] 00000000 00000001		STATR1 [R/W] 00000000 00000000		CAN 1 Control Register
$00C104_H$	ERRCNT1 [R] 00000000 00000000		BTR1 [R/W] 00100011 00000001		
$00C108_H$	INTR1 [R] 00000000 00000000		TESTR1 [R/W] 00000000 X0000000		
$00C10C_H$	BRPE1 [R/W] 00000000 00000000		CBSYNC1 *2		
$00C110_H$	IF1CREQ1 [R/W] 00000000 00000001		IF1CMSK1 [R/W] 00000000 00000000		CAN 1 IF 1 Register
$00C114_H$	IF1MSK21 [R/W] 11111111 11111111		IF1MSK11 [R/W] 11111111 11111111		

Address	Register				Block
	+0	+1	+2	+3	
$00C118_H$	IF1ARB21 [R/W] 00000000 00000000		IF1ARB11 [R/W] 00000000 00000000		
$00C11C_H$	IF1MCTR1 [R/W] 00000000 00000000		res.		
$00C120_H$	IF1DTA11 [R/W] 00000000 00000000		IF1DTA21 [R/W] 00000000 00000000		
$00C124_H$	IF1DTB11 [R/W] 00000000 00000000		IF1DTB21 [R/W] 00000000 00000000		
$00C128_H$ - $00C12C_H$	reserved				
$00C130_H$	*IF1DTA21 [R/W]* *00000000 00000000*		*IF1DTA11 [R/W]* *00000000 00000000*		
$00C134_H$	*IF1DTB21 [R/W]* *00000000 00000000*		*IF1DTB11 [R/W]* *00000000 00000000*		
$00C138_H$ - $00C13C_H$	reserved				
$00C140_H$	IF2CREQ1 [R/W] 00000000 00000001		IF2CMSK1 [R/W] 00000000 00000000		CAN 1 IF 2 Register
$00C144_H$	IF2MSK21 [R/W] 11111111 11111111		IF2MSK11 [R/W] 11111111 11111111		
$00C148_H$	IF2ARB21 [R/W] 00000000 00000000		IF2ARB11 [R/W] 00000000 00000000		

Address	Register				Block
	+0	+1	+2	+3	
$00C14C_H$	IF2MCTR1 [R/W] 00000000 00000000		res.		
$00C150_H$	IF2DTA11 [R/W] 00000000 00000000		IF2DTA21 [R/W] 00000000 00000000		
$00C154_H$	IF2DTB11 [R/W] 00000000 00000000		IF2DTB21 [R/W] 00000000 00000000		
$00C158_H$ - $00C15C_H$	reserved				
$00C160_H$	*IF2DTA21 [R/W]* *00000000 00000000*		*IF2DTA11 [R/W]* *00000000 00000000*		
$00C164_H$	*IF2DTB21 [R/W]* *00000000 00000000*		*IF2DTB11 [R/W]* *00000000 00000000*		
$00C168_H$ - $00C17C_H$	reserved				
$00C180_H$	TREQR21 [R] 00000000 00000000		TREQR11 [R] 00000000 00000000		CAN 1 Status Flags
$00C184_H$	~~TREQR41 [R]~~ ~~00000000 00000000~~		~~TREQR31 [R]~~ ~~00000000 00000000~~		
$00C188_H$	~~TREQR61 [R]~~ ~~00000000 00000000~~		~~TREQR51 [R]~~ ~~00000000 00000000~~		
$00C18C_H$	~~TREQR81 [R]~~ ~~00000000 00000000~~		~~TREQR71 [R]~~ ~~00000000 00000000~~		

Address	Register				Block
	+0	+1	+2	+3	
$00C190_H$	NEWDT21 [R] 00000000 00000000		NEWDT11 [R] 00000000 00000000		
$00C194_H$	~~NEWDT41 [R]~~ ~~00000000 00000000~~		~~NEWDT31 [R]~~ ~~00000000 00000000~~		
$00C198_H$	~~NEWDT61 [R]~~ ~~00000000 00000000~~		~~NEWDT51 [R]~~ ~~00000000 00000000~~		
$00C19C_H$	~~NEWDT81 [R]~~ ~~00000000 00000000~~		~~NEWDT71 [R]~~ ~~00000000 00000000~~		
$00C1A0_H$	INTPND21 [R] 00000000 00000000		INTPND11 [R] 00000000 00000000		
$00C1A4_H$	~~INTPND41 [R]~~ ~~00000000 00000000~~		~~INTPND31 [R]~~ ~~00000000 00000000~~		
$00C1A8_H$	~~INTPND61 [R]~~ ~~00000000 00000000~~		~~INTPND51 [R]~~ ~~00000000 00000000~~		
$00C1AC_H$	~~INTPND81 [R]~~ ~~00000000 00000000~~		~~INTPND71 [R]~~ ~~00000000 00000000~~		
$00C1B0_H$	MSGVAL21 [R] 00000000 00000000		MSGVAL11 [R] 00000000 00000000		
$00C1B4_H$	~~MSGVAL41 [R]~~ ~~00000000 00000000~~		~~MSGVAL31 [R]~~ ~~00000000 00000000~~		
$00C1B8_H$	~~MSGVAL61 [R]~~ ~~00000000 00000000~~		~~MSGVAL51 [R]~~ ~~00000000 00000000~~		

Address	Register				Block
	+0	+1	+2	+3	
00C1BC$_H$	~~MSGVAL81 [R]~~ ~~00000000 00000000~~		~~MSGVAL71 [R]~~ ~~00000000 00000000~~		
00C1C0$_H$ - 00C1FC$_H$	reserved				
00C200$_H$	CTRLR2 [R/W] 00000000 00000001		STATR2 [R/W] 00000000 00000000		CAN 2 Control Register
00C204$_H$	ERRCNT2 [R] 00000000 00000000		BTR2 [R/W] 00100011 00000001		
00C208$_H$	INTR2 [R] 00000000 00000000		TESTR2 [R/W] 00000000 X0000000		
00C20C$_H$	BRPE2 [R/W] 00000000 00000000		CBSYNC2 *2		
00C210$_H$	IF1CREQ2 [R/W] 00000000 00000001		IF1CMSK2 [R/W] 00000000 00000000		CAN 2 IF 1 Register
00C214$_H$	IF1MSK22 [R/W] 11111111 11111111		IF1MSK12 [R/W] 11111111 11111111		
00C218$_H$	IF1ARB22 [R/W] 00000000 00000000		IF1ARB12 [R/W] 00000000 00000000		
00C21C$_H$	IF1MCTR2 [R/W] 00000000 00000000		res.		
00C220$_H$	IF1DTA12 [R/W] 00000000 00000000		IF1DTA22 [R/W] 00000000 00000000		

Address	Register				Block
	+0	+1	+2	+3	
$00C224_H$	IF1DTB12 [R/W] 00000000 00000000		IF1DTB22 [R/W] 00000000 00000000		
$00C228_H$ - $00C22C_H$	reserved				
$00C230_H$	*IF1DTA22 [R/W]* *00000000 00000000*		*IF1DTA12 [R/W]* *00000000 00000000*		
$00C234_H$	*IF1DTB22 [R/W]* *00000000 00000000*		*IF1DTB12 [R/W]* *00000000 00000000*		
$00C238_H$ - $00C23C_H$	reserved				
$00C240_H$	IF2CREQ2 [R/W] 00000000 00000001		IF2CMSK2 [R/W] 00000000 00000000		CAN 2 IF 2 Register
$00C244_H$	IF2MSK22 [R/W] 11111111 11111111		IF2MSK12 [R/W] 11111111 11111111		
$00C248_H$	IF2ARB22 [R/W] 00000000 00000000		IF2ARB12 [R/W] 00000000 00000000		
$00C24C_H$	IF2MCTR2 [R/W] 00000000 00000000		res.		
$00C250_H$	IF2DTA12 [R/W] 00000000 00000000		IF2DTA22 [R/W] 00000000 00000000		
$00C254_H$	IF2DTB12 [R/W] 00000000 00000000		IF2DTB22 [R/W] 00000000 00000000		

Address	Register				Block
	+0	+1	+2	+3	
$00C258_H$ - $00C25C_H$	reserved				
$00C260_H$	*IF2DTA22 [R/W]* *00000000 00000000*		*IF2DTA12 [R/W]* *00000000 00000000*		
$00C264_H$	*IF2DTB22 [R/W]* *00000000 00000000*		*IF2DTB12 [R/W]* *00000000 00000000*		
$00C268_H$ - $00C27C_H$	reserved				
$00C280_H$	TREQR22 [R] 00000000 00000000		TREQR12 [R] 00000000 00000000		CAN 2 Status Flags
$00C284_H$	~~TREQR42 [R]~~ ~~00000000 00000000~~		~~TREQR32 [R]~~ ~~00000000 00000000~~		
$00C288_H$	~~TREQR62 [R]~~ ~~00000000 00000000~~		~~TREQR52 [R]~~ ~~00000000 00000000~~		
$00C28C_H$	~~TREQR82 [R]~~ ~~00000000 00000000~~		~~TREQR72 [R]~~ ~~00000000 00000000~~		
$00C290_H$	NEWDT22 [R] 00000000 00000000		NEWDT12 [R] 00000000 00000000		
$00C294_H$	~~NEWDT42 [R]~~ ~~00000000 00000000~~		~~NEWDT32 [R]~~ ~~00000000 00000000~~		
$00C298_H$	~~NEWDT62 [R]~~ ~~00000000 00000000~~		~~NEWDT52 [R]~~ ~~00000000 00000000~~		

Address	Register				Block
	+0	+1	+2	+3	
$00C29C_H$	~~NEWDT82 [R]~~ ~~00000000 00000000~~		~~NEWDT72 [R]~~ ~~00000000 00000000~~		
$00C2A0_H$	INTPND22 [R] 00000000 00000000		INTPND12 [R] 00000000 00000000		
$00C2A4_H$	~~INTPND42 [R]~~ ~~00000000 00000000~~		~~INTPND32 [R]~~ ~~00000000 00000000~~		
$00C2A8_H$	~~INTPND62 [R]~~ ~~00000000 00000000~~		~~INTPND52 [R]~~ ~~00000000 00000000~~		
$00C2AC_H$	~~INTPND82 [R]~~ ~~00000000 00000000~~		~~INTPND72 [R]~~ ~~00000000 00000000~~		
$00C2B0_H$	MSGVAL22 [R] 00000000 00000000		MSGVAL12 [R] 00000000 00000000		
$00C2B4_H$	~~MSGVAL42 [R]~~ ~~00000000 00000000~~		~~MSGVAL32 [R]~~ ~~00000000 00000000~~		
$00C2B8_H$	~~MSGVAL62 [R]~~ ~~00000000 00000000~~		~~MSGVAL52 [R]~~ ~~00000000 00000000~~		
$00C2BC_H$	~~MSGVAL82 [R]~~ ~~00000000 00000000~~		~~MSGVAL72 [R]~~ ~~00000000 00000000~~		
$00C2C0_H$ - $00C2FC_H$	reserved				
$00C300_H$	CTRLR3 [R/W] 00000000 00000001		STATR3 [R/W] 00000000 00000000		CAN 3 Control Register

Address	Register				Block
	+0	+1	+2	+3	
$00C304_H$	ERRCNT3 [R] 00000000 00000000		BTR3 [R/W] 00100011 00000001		
$00C308_H$	INTR3 [R] 00000000 00000000		TESTR3 [R/W] 00000000 X0000000		
$00C30C_H$	BRPE3 [R/W] 00000000 00000000		CBSYNC3 *2		
$00C310_H$	IF1CREQ3 [R/W] 00000000 00000001		IF1CMSK3 [R/W] 00000000 00000000		CAN 3 IF 1 Register
$00C314_H$	IF1MSK23 [R/W] 11111111 11111111		IF1MSK13 [R/W] 11111111 11111111		
$00C318_H$	IF1ARB23 [R/W] 00000000 00000000		IF1ARB13 [R/W] 00000000 00000000		
$00C31C_H$	IF1MCTR3 [R/W] 00000000 00000000		res.		
$00C320_H$	IF1DTA13 [R/W] 00000000 00000000		IF1DTA23 [R/W] 00000000 00000000		
$00C324_H$	IF1DTB13 [R/W] 00000000 00000000		IF1DTB23 [R/W] 00000000 00000000		
$00C328_H$ - $00C32C_H$	reserved				
$00C330_H$	*IF1DTA23 [R/W]* *00000000 00000000*		*IF1DTA13 [R/W]* *00000000 00000000*		

Address	Register				Block
	+0	+1	+2	+3	
$00C334_H$	*IF1DTB23 [R/W]* *00000000 00000000*		*IF1DTB13 [R/W]* *00000000 00000000*		
$00C338_H$ - $00C33C_H$	reserved				
$00C340_H$	IF2CREQ3 [R/W] 00000000 00000001		IF2CMSK3 [R/W] 00000000 00000000		CAN 3 IF 2 Register
$00C344_H$	IF2MSK23 [R/W] 11111111 11111111		IF2MSK13 [R/W] 11111111 11111111		
$00C348_H$	IF2ARB23 [R/W] 00000000 00000000		IF2ARB13 [R/W] 00000000 00000000		
$00C34C_H$	IF2MCTR3 [R/W] 00000000 00000000		res.		
$00C350_H$	IF2DTA13 [R/W] 00000000 00000000		IF2DTA23 [R/W] 00000000 00000000		
$00C354_H$	IF2DTB13 [R/W] 00000000 00000000		IF2DTB23 [R/W] 00000000 00000000		
$00C358_H$ - $00C35C_H$	reserved				
$00C360_H$	*IF2DTA23 [R/W]* *00000000 00000000*		*IF2DTA13 [R/W]* *00000000 00000000*		
$00C364_H$	*IF2DTB23 [R/W]* *00000000 00000000*		*IF2DTB13 [R/W]* *00000000 00000000*		

Address	Register				Block
	+0	+1	+2	+3	
$00C368_H$ - $00C37C_H$	reserved				
$00C380_H$	TREQR23 [R] 00000000 00000000		TREQR13 [R] 00000000 00000000		CAN 3 Status Flags
$00C384_H$	~~TREQR43 [R] 00000000 00000000~~		~~TREQR33 [R] 00000000 00000000~~		
$00C388_H$	~~TREQR63 [R] 00000000 00000000~~		~~TREQR53 [R] 00000000 00000000~~		
$00C38C_H$	~~TREQR83 [R] 00000000 00000000~~		~~TREQR73 [R] 00000000 00000000~~		
$00C390_H$	NEWDT23 [R] 00000000 00000000		NEWDT13 [R] 00000000 00000000		
$00C394_H$	~~NEWDT43 [R] 00000000 00000000~~		~~NEWDT33 [R] 00000000 00000000~~		
$00C398_H$	~~NEWDT63 [R] 00000000 00000000~~		~~NEWDT53 [R] 00000000 00000000~~		
$00C39C_H$	~~NEWDT83 [R] 00000000 00000000~~		~~NEWDT73 [R] 00000000 00000000~~		
$00C3A0_H$	INTPND23 [R] 00000000 00000000		INTPND13 [R] 00000000 00000000		
$00C3A4_H$	~~INTPND43 [R] 00000000 00000000~~		~~INTPND33 [R] 00000000 00000000~~		

Address	Register				Block
	+0	+1	+2	+3	
$00C3A8_H$	~~INTPND63 [R]~~ ~~00000000 00000000~~		~~INTPND53 [R]~~ ~~00000000 00000000~~		
$00C3AC_H$	~~INTPND83 [R]~~ ~~00000000 00000000~~		~~INTPND73 [R]~~ ~~00000000 00000000~~		
$00C3B0_H$	MSGVAL23 [R] 00000000 00000000		MSGVAL13 [R] 00000000 00000000		
$00C3B4_H$	~~MSGVAL43 [R]~~ ~~00000000 00000000~~		~~MSGVAL33 [R]~~ ~~00000000 00000000~~		
$00C3B8_H$	~~MSGVAL63 [R]~~ ~~00000000 00000000~~		~~MSGVAL53 [R]~~ ~~00000000 00000000~~		
$00C3BC_H$	~~MSGVAL83 [R]~~ ~~00000000 00000000~~		~~MSGVAL73 [R]~~ ~~00000000 00000000~~		
$00C3C0_H$ - $00C3FC_H$	reserved				
$00C400_H$	CTRLR4 [R/W] 00000000 00000001		STATR4 [R/W] 00000000 00000000		CAN 4 Control Register
$00C404_H$	ERRCNT4 [R] 00000000 00000000		BTR4 [R/W] 00100011 00000001		
$00C408_H$	INTR4 [R] 00000000 00000000		TESTR4 [R/W] 00000000 X0000000		
$00C40C_H$	BRPE4 [R/W] 00000000 00000000		CBSYNC4 *2		

Address	Register				Block
	+0	+1	+2	+3	
$00C410_H$	IF1CREQ4 [R/W] 00000000 00000001		IF1CMSK4 [R/W] 00000000 00000000		CAN 4 IF 1 Register
$00C414_H$	IF1MSK24 [R/W] 11111111 11111111		IF1MSK14 [R/W] 11111111 11111111		
$00C418_H$	IF1ARB24 [R/W] 00000000 00000000		IF1ARB14 [R/W] 00000000 00000000		
$00C41C_H$	IF1MCTR4 [R/W] 00000000 00000000		res.		
$00C420_H$	IF1DTA14 [R/W] 00000000 00000000		IF1DTA24 [R/W] 00000000 00000000		
$00C424_H$	IF1DTB14 [R/W] 00000000 00000000		IF1DTB24 [R/W] 00000000 00000000		
$00C428_H$ - $00C42C_H$	reserved				
$00C430_H$	*IF1DTA24 [R/W]* *00000000 00000000*		*IF1DTA14 [R/W]* *00000000 00000000*		
$00C434_H$	*IF1DTB24 [R/W]* *00000000 00000000*		*IF1DTB14 [R/W]* *00000000 00000000*		
$00C438_H$ - $00C43C_H$	reserved				
$00C440_H$	IF2CREQ4 [R/W] 00000000 00000001		IF2CMSK4 [R/W] 00000000 00000000		CAN 4 IF 2 Register

Address	Register				Block
	+0	+1	+2	+3	
$00C444_H$	IF2MSK24 [R/W] 11111111 11111111		IF2MSK14 [R/W] 11111111 11111111		
$00C448_H$	IF2ARB24 [R/W] 00000000 00000000		IF2ARB14 [R/W] 00000000 00000000		
$00C44C_H$	IF2MCTR4 [R/W] 00000000 00000000		res.		
$00C450_H$	IF2DTA14 [R/W] 00000000 00000000		IF2DTA24 [R/W] 00000000 00000000		
$00C454_H$	IF2DTB14 [R/W] 00000000 00000000		IF2DTB24 [R/W] 00000000 00000000		
$00C458_H$ - $00C45C_H$	reserved				
$00C460_H$	*IF2DTA24 [R/W]* *00000000 00000000*		*IF2DTA14 [R/W]* *00000000 00000000*		
$00C464_H$	*IF2DTB24 [R/W]* *00000000 00000000*		*IF2DTB14 [R/W]* *00000000 00000000*		
$00C468_H$ - $00C47C_H$	reserved				
$00C480_H$	TREQR24 [R] 00000000 00000000		TREQR14 [R] 00000000 00000000		CAN 4 Status Flags
$00C484_H$	~~TREQR44 [R]~~ ~~00000000 00000000~~		~~TREQR34 [R]~~ ~~00000000 00000000~~		

Address	Register				Block
	+0	+1	+2	+3	
00C488$_H$	~~TREQR64 [R]~~ ~~00000000 00000000~~		~~TREQR54 [R]~~ ~~00000000 00000000~~		
00C48C$_H$	~~TREQR84 [R]~~ ~~00000000 00000000~~		~~TREQR74 [R]~~ ~~00000000 00000000~~		
00C490$_H$	NEWDT24 [R] 00000000 00000000		NEWDT14 [R] 00000000 00000000		
00C494$_H$	~~NEWDT44 [R]~~ ~~00000000 00000000~~		~~NEWDT34 [R]~~ ~~00000000 00000000~~		
00C498$_H$	~~NEWDT64 [R]~~ ~~00000000 00000000~~		~~NEWDT54 [R]~~ ~~00000000 00000000~~		
00C49C$_H$	~~NEWDT84 [R]~~ ~~00000000 00000000~~		~~NEWDT74 [R]~~ ~~00000000 00000000~~		
00C4A0$_H$	INTPND24 [R] 00000000 00000000		INTPND14 [R] 00000000 00000000		
00C4A4$_H$	~~INTPND44 [R]~~ ~~00000000 00000000~~		~~INTPND34 [R]~~ ~~00000000 00000000~~		
00C4A8$_H$	~~INTPND64 [R]~~ ~~00000000 00000000~~		~~INTPND54 [R]~~ ~~00000000 00000000~~		
00C4AC$_H$	~~INTPND84 [R]~~ ~~00000000 00000000~~		~~INTPND74 [R]~~ ~~00000000 00000000~~		
00C4B0$_H$	MSGVAL24 [R] 00000000 00000000		MSGVAL14 [R] 00000000 00000000		

Address	Register				Block
	+0	+1	+2	+3	
$00C4B4_H$	~~MSGVAL44 [R]~~ ~~00000000 00000000~~		~~MSGVAL34 [R]~~ ~~00000000 00000000~~		
$00C4B8_H$	~~MSGVAL64 [R]~~ ~~00000000 00000000~~		~~MSGVAL54 [R]~~ ~~00000000 00000000~~		
$00C4BC_H$	~~MSGVAL84 [R]~~ ~~00000000 00000000~~		~~MSGVAL74 [R]~~ ~~00000000 00000000~~		
$00C4C0_H$ - $00C4FC_H$	reserved				
$00C500_H$	CTRLR5 [R/W] 00000000 00000001		STATR5 [R/W] 00000000 00000000		CAN 5 Control Register
$00C504_H$	ERRCNT5 [R] 00000000 00000000		BTR5 [R/W] 00100011 00000001		
$00C508_H$	INTR5 [R] 00000000 00000000		TESTR5 [R/W] 00000000 X0000000		
$00C50C_H$	BRPE5 [R/W] 00000000 00000000		CBSYNC5 *2		
$00C510_H$	IF1CREQ5 [R/W] 00000000 00000001		IF1CMSK5 [R/W] 00000000 00000000		CAN 5 IF 1 Register
$00C514_H$	IF1MSK25 [R/W] 11111111 11111111		IF1MSK15 [R/W] 11111111 11111111		
$00C518_H$	IF1ARB25 [R/W] 00000000 00000000		IF1ARB15 [R/W] 00000000 00000000		

Address	Register				Block
	+0	+1	+2	+3	
$00C51C_H$	IF1MCTR5 [R/W] 00000000 00000000		res.		
$00C520_H$	IF1DTA15 [R/W] 00000000 00000000		IF1DTA25 [R/W] 00000000 00000000		
$00C524_H$	IF1DTB15 [R/W] 00000000 00000000		IF1DTB25 [R/W] 00000000 00000000		
$00C528_H$ - $00C52C_H$	reserved				
$00C530_H$	*IF1DTA25 [R/W]* *00000000 00000000*		*IF1DTA15 [R/W]* *00000000 00000000*		
$00C534_H$	*IF1DTB25 [R/W]* *00000000 00000000*		*IF1DTB15 [R/W]* *00000000 00000000*		
$00C538_H$ - $00C53C_H$	reserved				
$00C540_H$	IF2CREQ5 [R/W] 00000000 00000001		IF2CMSK5 [R/W] 00000000 00000000		CAN 5 IF 2 Register
$00C544_H$	IF2MSK25 [R/W] 11111111 11111111		IF2MSK15 [R/W] 11111111 11111111		
$00C548_H$	IF2ARB25 [R/W] 00000000 00000000		IF2ARB15 [R/W] 00000000 00000000		
$00C54C_H$	IF2MCTR5 [R/W] 00000000 00000000		res.		

Address	Register				Block
	+0	+1	+2	+3	
$00C550_H$	IF2DTA15 [R/W] 00000000 00000000		IF2DTA25 [R/W] 00000000 00000000		
$00C554_H$	IF2DTB15 [R/W] 00000000 00000000		IF2DTB25 [R/W] 00000000 00000000		
$00C558_H$ - $00C55C_H$	reserved				
$00C560_H$	*IF2DTA25 [R/W]* *00000000 00000000*		*IF2DTA15 [R/W]* *00000000 00000000*		
$00C564_H$	*IF2DTB25 [R/W]* *00000000 00000000*		*IF2DTB15 [R/W]* *00000000 00000000*		
$00C568_H$ - $00C57C_H$	reserved				
$00C580_H$	TREQR25 [R] 00000000 00000000		TREQR15 [R] 00000000 00000000		CAN 5 Status Flags
$00C584_H$	~~TREQR45 [R]~~ ~~00000000 00000000~~		~~TREQR35 [R]~~ ~~00000000 00000000~~		
$00C588_H$	~~TREQR65 [R]~~ ~~00000000 00000000~~		~~TREQR55 [R]~~ ~~00000000 00000000~~		
$00C58C_H$	~~TREQR85 [R]~~ ~~00000000 00000000~~		~~TREQR75 [R]~~ ~~00000000 00000000~~		
$00C590_H$	NEWDT25 [R] 00000000 00000000		NEWDT15 [R] 00000000 00000000		

Address	Register				Block
	+0	+1	+2	+3	
00C594$_H$	~~NEWDT45 [R]~~ ~~00000000 00000000~~		~~NEWDT35 [R]~~ ~~00000000 00000000~~		
00C598$_H$	~~NEWDT65 [R]~~ ~~00000000 00000000~~		~~NEWDT55 [R]~~ ~~00000000 00000000~~		
00C59C$_H$	~~NEWDT85 [R]~~ ~~00000000 00000000~~		~~NEWDT75 [R]~~ ~~00000000 00000000~~		
00C5A0$_H$	INTPND25 [R] 00000000 00000000		INTPND15 [R] 00000000 00000000		
00C5A4$_H$	~~INTPND45 [R]~~ ~~00000000 00000000~~		~~INTPND35 [R]~~ ~~00000000 00000000~~		
00C5A8$_H$	~~INTPND65 [R]~~ ~~00000000 00000000~~		~~INTPND55 [R]~~ ~~00000000 00000000~~		
00C5AC$_H$	~~INTPND85 [R]~~ ~~00000000 00000000~~		~~INTPND75 [R]~~ ~~00000000 00000000~~		
00C5B0$_H$	MSGVAL25 [R] 00000000 00000000		MSGVAL15 [R] 00000000 00000000		
00C5B4$_H$	~~MSGVAL45 [R]~~ ~~00000000 00000000~~		~~MSGVAL35 [R]~~ ~~00000000 00000000~~		
00C5B8$_H$	~~MSGVAL65 [R]~~ ~~00000000 00000000~~		~~MSGVAL55 [R]~~ ~~00000000 00000000~~		
00C5BC$_H$	~~MSGVAL85 [R]~~ ~~00000000 00000000~~		~~MSGVAL75 [R]~~ ~~00000000 00000000~~		

Address	Register				Block
	+0	+1	+2	+3	
$00C5C0_H$ - $00EFFC_H$	reserved				
$00F000_H$	BCTRL [R/W] -------- -------- 11111100 00000000				EDSU / MPU
$00F004_H$	BSTAT [R/W] -------- -----000 00000000 10--000000				
$00F008_H$	BIAC [R] -------- -------- 00000000 00000000				
$00F00C_H$	BOAC [R] -------- -------- 00000000 00000000				
$00F010_H$	BIRQ [R/W] -------- -------- 00000000 00000000				
$00F014_H$ - $00F01C_H$	reserved				
$00F020_H$	BCR0 [R/W] -------- 00000000 00000000 00000000				
$00F024_H$	BCR1 [R/W] -------- 00000000 00000000 00000000				
$00F028_H$	BCR2 [R/W] -------- 00000000 00000000 00000000				
$00F02C_H$	BCR3 [R/W] -------- 00000000 00000000 00000000				
$00F030_H$	~~BCR4 [R/W]~~				

Address	Register				Block
	+0	+1	+2	+3	
$00F034_H$	~~BCR5 [R/W]~~				
$00F038_H$	~~BCR6 [R/W]~~				
$00F03C_H$	~~BCR7 [R/W]~~				
$00F040_H$ - $00F07C_H$	reserved				
$00F080_H$	BAD0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				EDSU / MPU
$00F084_H$	BAD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F088_H$	BAD2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F08C_H$	BAD3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F090_H$	BAD4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F094_H$	BAD5 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F098_H$	BAD6 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F09C_H$	BAD7 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0A0_H$	BAD8 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Register				Block
	+0	+1	+2	+3	
$00F0A4_H$	BAD9 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0A8_H$	BAD10 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0AC_H$	BAD11 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0B0_H$	BAD12 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0B4_H$	BAD13 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0B8_H$	BAD14 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0BC_H$	BAD15 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0C0_H$	~~BAD16 [R/W]~~				EDSU / MPU
$00F0C4_H$	~~BAD17 [R/W]~~				
$00F0C8_H$	~~BAD18 [R/W]~~				
$00F0CC_H$	~~BAD19 [R/W]~~				
$00F0D0_H$	~~BAD20 [R/W]~~				
$00F0D4_H$	~~BAD21 [R/W]~~				

Address	Register				Block
	+0	+1	+2	+3	
$00F0D8_H$	~~BAD22 [R/W]~~				
$00F0DC_H$	~~BAD23 [R/W]~~				
$00F0E0_H$	~~BAD24 [R/W]~~				
$00F0E4_H$	~~BAD25 [R/W]~~				
$00F0E8_H$	~~BAD26 [R/W]~~				
$00F0EC_H$	~~BAD27 [R/W]~~				
$00F0F0_H$	~~BAD28 [R/W]~~				
$00F0F4_H$	~~BAD29 [R/W]~~				
$00F0F8_H$	~~BAD30 [R/W]~~				
$00F0FC_H$	~~BAD31 [R/W]~~				
$00F100_H$ - $00FFFC_H$	reserved				
010000_H - $013FFC_H$	~~Cache TAG way 1 (010000_H – $0107FC_H$)~~				~~2 way set associative I-Cache 4kB~~

Address	Register				Block
	+0	+1	+2	+3	
014000_H - $017FFC_H$	~~Cache TAG way 2 (014000_H – $0147FC_H$)~~				
018000_H - $01BFFC_H$	~~Cache RAM way 1 (018000_H – $0187FC_H$)~~				
$01C000_H$ - $01FFFC_H$	~~Cache RAM way 2 ($01C000_H$ – $01C7FC_H$)~~				
020000_H - $02FFFC_H$	***MB91F467BA/466BA/465BA/464BA D-RAM size is 24kB : $02A000_H$ - $02FFFC_H$*** (data access is 0 waitcycles)				DBUS-RAM 24 kB
030000_H - $03FFFC_H$	***MB91F467BA/466BA/465BA/464BA I-/D-RAM size is 16kB : 030000_H - $033FFC_H$*** (instruction access is 0 waitcycles, data access is 1 waitcycle)				GP-RAM (FLASHIF) 16 kB
040000_H - $05FFFC_H$	ROMS00 area (128kB) ***MB91F465BA/464BA : Not available in this area***				**MB91F467BA** Flash Memory (1024kB + 64kB) **MB91F466BA** Flash Memory (768kB + 64kB) **MB91F465BA** Flash Memory (512kB + 32kB) **MB91F464BA** Flash Memory (384kB + 32kB)
060000_H - $07FFFC_H$	ROMS01 area (128kB) ***MB91F465BA/464BA : Not available in this area***				
080000_H - $09FFFC_H$	ROMS02 area (128kB) ***MB91F464BA : Not available in this area***				
$0A0000_H$ - $0BFFFC_H$	ROMS03 area (128kB)				
$0C0000_H$ - $0DFFFC_H$	ROMS04 area (128kB)				

Address	Register				Block
	+0	+1	+2	+3	
$0E0000_H$ - $0FFFF4_H$	ROMS05 area (128kB)				
$0FFFF8_H$	FMV [R] $06\ 00\ 00\ 00_H$				Fixed Reset/Mode Vector
$0FFFFC_H$	FRV [R] $00\ 00\ BF\ F8_H$				
100000_H - $13FFFC_H$	ROMS06 area (256kB) ***MB91F466BA/465BA/464BA : Not available in this area***				**MB91F467BA** Flash Memory (1024kB + 64kB) **MB91F466BA** Flash Memory (768kB + 64kB) **MB91F465BA** Flash Memory (512kB + 32kB) **MB91F464BA** Flash Memory (384kB + 32kB)
140000_H - $17FFFC_H$	ROMS07 area (256kB) ***MB91F467BA/466BA ROMS07 size is 64kB : 140000_H - $14FFFC_H$*** ***MB91F465BA/464BA ROMS07 size is 32kB : 148000_H - $14FFFC_H$***				
180000_H - $1BFFFC_H$	~~***ROMS08 area (256kB)***~~				Ext. bus
$1C0000_H$ - $1FFFFC_H$	~~***ROMS09 area (256kB)***~~				
200000_H - $27FFFC_H$	~~***ROMS10 area (512kB)***~~				
280000_H - $3FFFFC_H$	~~***ROMS11 area (512kB) - ROMS13 area (512kB)***~~				

Address	Register				Block
	+0	+1	+2	+3	
~~400000$_H$ = 4FFFFC$_H$~~	~~***ROMS14 area (512kB) - ROMS15 area (512kB)***~~				
~~500000$_H$ = FFFFFC$_H$~~	Ext. bus				

- Write operations to address 0FFFF8$_H$ and 0FFFFC$_H$ are not possible. When reading these addresses, the values shown above will be read.
- Flash Security Vectors are located as follows:
  FSV1: 0x0014:8000 BSV1: 0x0014:8004
  FSV2: 0x0014:8008 BSV2: 0x0014:800C

*1 Use a read access (byte or halfword) to this address to synchronize the CPU operation (e.g. the interrupt acceptanceof the CPU) to a preceding write access to the resources on R-bus (e.g. to an interrupt flag) on followingaddresses (0x0000-0x01FF, 0x0280-0x037F, 0x0400-0x063F and 0x0C00-0x0FFF).

*2 Use a read access (byte or halfword) to this address to synchronize the CPU operation (e.g. the interrupt acceptance of the CPU) to a preceding write access to the CANs on D-bus (e.g. to an interrupt flag) on following addresses (0xC000-0xFFFF).

Note:

***3 EIRR makes valid after write to ELVR.**

When you want to write to EIRR just after write to ELVR, you must write to EIRR after dummy read ELVR.

Note: reserved areas shall not be used at all

5 Interrupt Vector Table

This section shows the allocation of interrupts and interrupt vector/interrupt register.

Interrupt	Interrupt number		Interuupt level[*1]		Interuupt vector[*2]		RN
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	
Reset	0	00	-	-	0x3FC	0x000FFFFC	
Mode vector	1	01	-	-	0x3F8	0x000FFFF8	
System reserved	2	02	-	-	0x3F4	0x000FFFF4	
System reserved	3	03	-	-	0x3F0	0x000FFFF0	
System reserved	4	04	-	-	0x3EC	0x000FFFEC	
CPU supervisor mode (INT #5 instruction) [*6]	5	05	-	-	0x3E8	0x000FFFE8	
Memory Protection exception [*6]	6	06	-	-	0x3E4	0x000FFFE4	
Co-processor fault trap [*5]	7	07	-	-	0x3E0	0x000FFFE0	
Co-processor error trap [*5]	8	08	-	-	0x3DC	0x000FFFDC	
INTE instruction [*5]	9	09	-	-	0x3D8	0x000FFFD8	
Instruction break	10	0A	-	-	0x3D4	0x000FFFD4	
Operand break trap [*5]	11	0B	-	-	0x3D0	0x000FFFD0	
Step trace trap [*5]	12	0C	-	-	0x3CC	0x000FFFCC	
NMI interrupt (tool)[*5]	13	0D	-	-	0x3C8	0x000FFFC8	
Undefined instruction	14	0E	-	-	0x3C4	0x000FFFC4	
NMI request	15	0F	F_H fixed		0x3C0	0x000FFFC0	
External Interrupt 0	16	10	ICR00	0x440	0x3BC	0x000FFFBC	0, 16
External Interrupt 1	17	11			0x3B8	0x000FFFB8	1, 17

Interrupt	Interrupt number		Interuupt level[*1]		Interuupt vector[*2]		RN
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	
External Interrupt 2	18	12	ICR01	0x441	0x3B4	0x000FFFB4	2, 18
External Interrupt 3	19	13			0x3B0	0x000FFFB0	3, 19
External Interrupt 4	20	14	ICR02	0x442	0x3AC	0x000FFFAC	20
External Interrupt 5	21	15			0x3A8	0x000FFFA8	21
External Interrupt 6	22	16	ICR03	0x443	0x3A4	0x000FFFA4	22
External Interrupt 7	23	17			0x3A0	0x000FFFA0	23
External Interrupt 8	24	18	ICR04	0x444	0x39C	0x000FFF9C	
External Interrupt 9	25	19			0x398	0x000FFF98	
External Interrupt 10	26	1A	ICR05	0x445	0x394	0x000FFF94	
External Interrupt 11	27	1B			0x390	0x000FFF90	
External Interrupt 12	28	1C	ICR06	0x446	0x38C	0x000FFF8C	
External Interrupt 13	29	1D			0x388	0x000FFF88	
External Interrupt 14	30	1E	ICR07	0x447	0x384	0x000FFF84	
External Interrupt 15	31	1F			0x380	0x000FFF80	
Reload Timer 0	32	20	ICR08	0x448	0x37C	0x000FFF7C	4, 32
Reload Timer 1	33	21			0x378	0x000FFF78	5, 33
Reload Timer 2	34	22	ICR09	0x449	0x374	0x000FFF74	34
Reload Timer 3	35	23			0x370	0x000FFF70	35
Reload Timer 4	36	24	ICR10	0x44A	0x36C	0x000FFF6C	36
Reload Timer 5	37	25			0x368	0x000FFF68	37

Interrupt	Interrupt number		Interuupt level[*1]		Interuupt vector[*2]		RN
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	
Reload Timer 6	38	26	ICR11	0x44B	0x364	0x000FFF64	38
Reload Timer 7	39	27			0x360	0x000FFF60	39
Free Run Timer 0	40	28	ICR12	0x44C	0x35C	0x000FFF5C	40
Free Run Timer 1	41	29			0x358	0x000FFF58	41
Free Run Timer 2	42	2A	ICR13	0x44D	0x354	0x000FFF54	42
Free Run Timer 3	43	2B			0x350	0x000FFF50	43
Free Run Timer 4	44	2C	ICR14	0x44E	0x34C	0x000FFF4C	44
Free Run Timer 5	45	2D			0x348	0x000FFF48	45
Free Run Timer 6	46	2E	ICR15	0x44F	0x344	0x000FFF44	46
Free Run Timer 7	47	2F			0x340	0x000FFF40	47
CAN 0	48	30	ICR16	0x450	0x33C	0x000FFF3C	
CAN 1	49	31			0x338	0x000FFF38	
CAN 2	50	32	ICR17	0x451	0x334	0x000FFF34	
CAN 3	51	33			0x330	0x000FFF30	
CAN 4	52	34	ICR18	0x452	0x32C	0x000FFF2C	
CAN 5	53	35			0x328	0x000FFF28	
USART (LIN) 0 RX	54	36	ICR19	0x453	0x324	0x000FFF24	6, 48
USART (LIN) 0 TX	55	37			0x320	0x000FFF20	7, 49
reserved	56	38	ICR20	0x454	0x31C	0x000FFF1C	8, 50
reserved	57	39			0x318	0x000FFF18	9, 51

Interrupt	Interrupt number		Interuupt level[*1]		Interuupt vector[*2]		RN
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	
USART (LIN) 2 RX	58	3A	ICR21	0x455	0x314	0x000FFF14	52
USART (LIN) 2 TX	59	3B			0x310	0x000FFF10	53
USART (LIN) 3 RX	60	3C	ICR22	0x456	0x30C	0x000FFF0C	54
USART (LIN) 3 TX	61	3D			0x308	0x000FFF08	55
System reserved	62	3E	ICR23 [*4]	0x457	0x304	0x000FFF04	
Delayed Interrupt	63	3F			0x300	0x000FFF00	
System reserved [*3]	64	40	(ICR24)	(0x458)	0x2FC	0x000FFEFC	
System reserved [*3]	65	41			0x2F8	0x000FFEF8	
USART (LIN, FIFO) 4 RX	66	42	ICR25	0x459	0x2F4	0x000FFEF4	10, 56
USART (LIN, FIFO) 4 TX	67	43			0x2F0	0x000FFEF0	11, 57
USART (LIN, FIFO) 5 RX	68	44	ICR26	0x45A	0x2EC	0x000FFEEC	12, 58
USART (LIN, FIFO) 5 TX	69	45			0x2E8	0x000FFEE8	13, 59
USART (LIN, FIFO) 6 RX	70	46	ICR27	0x45B	0x2E4	0x000FFEE4	60
USART (LIN, FIFO) 6 TX	71	47			0x2E0	0x000FFEE0	61
USART (LIN, FIFO) 7 RX	72	48	ICR28	0x45C	0x2DC	0x000FFEDC	62
USART (LIN, FIFO) 7 TX	73	49			0x2D8	0x000FFED8	63
I2C 0	74	4A	ICR29	0x45D	0x2D4	0x000FFED4	
I2C 1	75	4B			0x2D0	0x000FFED0	
reserved	76	4C	ICR30	0x45E	0x2CC	0x000FFECC	64
reserved	77	4D			0x2C8	0x000FFEC8	65

Interrupt	Interrupt number		Interuupt level[*1]		Interuupt vector[*2]		RN
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	
reserved	78	4E	ICR31	0x45F	0x2C4	0x000FFEC4	66
reserved	79	4F			0x2C0	0x000FFEC0	67
reserved	80	50	ICR32	0x460	0x2BC	0x000FFEBC	68
reserved	81	51			0x2B8	0x000FFEB8	69
reserved	82	52	ICR33	0x461	0x2B4	0x000FFEB4	70
reserved	83	53			0x2B0	0x000FFEB0	71
reserved	84	54	ICR34	0x462	0x2AC	0x000FFEAC	72
reserved	85	55			0x2A8	0x000FFEA8	73
reserved	86	56	ICR35	0x463	0x2A4	0x000FFEA4	74
reserved	87	57			0x2A0	0x000FFEA0	75
reserved	88	58	ICR36	0x464	0x29C	0x000FFE9C	76
reserved	89	59			0x298	0x000FFE98	77
reserved	90	5A	ICR37	0x465	0x294	0x000FFE94	78
reserved	91	5B			0x290	0x000FFE90	79
Input Capture 0	92	5C	ICR38	0x466	0x28C	0x000FFE8C	80
Input Capture 1	93	5D			0x288	0x000FFE88	81
Input Capture 2	94	5E	ICR39	0x467	0x284	0x000FFE84	82
Input Capture 3	95	5F			0x280	0x000FFE80	83
Input Capture 4	96	60	ICR40	0x468	0x27C	0x000FFE7C	84
Input Capture 5	97	61			0x278	0x000FFE78	85

Interrupt	Interrupt number		Interuupt level[*1]		Interuupt vector[*2]		RN
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	
Input Capture 6	98	62	ICR41	0x469	0x274	0x000FFE74	86
Input Capture 7	99	63			0x270	0x000FFE70	87
Output Compare 0	100	64	ICR42	0x46A	0x26C	0x000FFE6C	88
Output Compare 1	101	65			0x268	0x000FFE68	89
Output Compare 2	102	66	ICR43	0x46B	0x264	0x000FFE64	90
Output Compare 3	103	67			0x260	0x000FFE60	91
Output Compare 4	104	68	ICR44	0x46C	0x25C	0x000FFE5C	92
Output Compare 5	105	69			0x258	0x000FFE58	93
Output Compare 6	106	6A	ICR45	0x46D	0x254	0x000FFE54	94
Output Compare 7	107	6B			0x250	0x000FFE50	95
Sound Generator	108	6C	ICR46	0x46E	0x24C	0x000FFE4C	
reserved	109	6D			0x248	0x000FFE48	
System reserved	110	6E	ICR47 [*4]	0x46F	0x244	0x000FFE44	
System reserved	111	6F			0x240	0x000FFE40	
Prog. Pulse Gen. 0	112	70	ICR48	0x470	0x23C	0x000FFE3C	15, 96
Prog. Pulse Gen. 1	113	71			0x238	0x000FFE38	97
Prog. Pulse Gen. 2	114	72	ICR49	0x471	0x234	0x000FFE34	98
Prog. Pulse Gen. 3	115	73			0x230	0x000FFE30	99
Prog. Pulse Gen. 4	116	74	ICR50	0x472	0x22C	0x000FFE2C	100
Prog. Pulse Gen. 5	117	75			0x228	0x000FFE28	101

Interrupt	Interrupt number		Interuupt level[*1]		Interuupt vector[*2]		RN
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	
Prog. Pulse Gen. 6	118	76	ICR51	0x473	0x224	0x000FFE24	102
Prog. Pulse Gen. 7	119	77			0x220	0x000FFE20	103
Prog. Pulse Gen. 8	120	78	ICR52	0x474	0x21C	0x000FFE1C	104
Prog. Pulse Gen. 9	121	79			0x218	0x000FFE18	105
Prog. Pulse Gen. 10	122	7A	ICR53	0x475	0x214	0x000FFE14	106
Prog. Pulse Gen. 11	123	7B			0x210	0x000FFE10	107
Prog. Pulse Gen. 12	124	7C	ICR54	0x476	0x20C	0x000FFE0C	108
Prog. Pulse Gen. 13	125	7D			0x208	0x000FFE08	109
Prog. Pulse Gen. 14	126	7E	ICR55	0x477	0x204	0x000FFE04	110
Prog. Pulse Gen. 15	127	7F			0x200	0x000FFE00	111
Up/Down Counter 0	128	80	ICR56	0x478	0x1FC	0x000FFDFC	
Up/Down Counter 1	129	81			0x1F8	0x000FFDF8	
reserved	130	82	ICR57	0x479	0x1F4	0x000FFDF4	
reserved	131	83			0x1F0	0x000FFDF0	
Real Time Clock	132	84	ICR58	0x47A	0x1EC	0x000FFDEC	
Calibration Unit	133	85			0x1E8	0x000FFDE8	
A/D Converter 0	134	86	ICR59	0x47B	0x1E4	0x000FFDE4	14, 112
-	135	87			0x1E0	0x000FFDE0	
Alarm Comparator 0	136	88	ICR60	0x47C	0x1DC	0x000FFDDC	
reserved	137	89			0x1D8	0x000FFDD8	

Interrupt	Interrupt number		Interuupt level[*1]		Interuupt vector[*2]		RN
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	
Low Voltage Detection	138	8A	ICR61	0x47D	0x1D4	0x000FFDD4	
reserved	139	8B			0x1D0	0x000FFDD0	
Time base Overflow	140	8C	ICR62	0x47E	0x1CC	0x000FFDCC	
PLL Clock Gear	141	8D			0x1C8	0x000FFDC8	
DMA Controller	142	8E	ICR63	0x47F	0x1C4	0x000FFDC4	
Main/Sub OSC stability wait	143	8F			0x1C0	0x000FFDC0	
Security vector	144	90	-	-	0x1BC	0x000FFDBC	
Used by the INT instruction.	145 to 255	91 to FF	-	-	0x1B8 to 0x000	0x000FFDB8 to 0x000FFC00	

Notes:

[*1] The ICRs are located in the interrupt controller and set the interrupt level for each interrupt request. An ICR is provided for each interrupt request.
[*2] The vector address for each EIT (exception, interrupt or trap) is calculated by adding the listed offset to the table base register value (TBR). The TBR specifies the top of the EIT vector table. The addresses listed in the table are for the default TBR value (0x000FFC00). The TBR is initialized to this value by a reset. After execution of the internal boot ROM TBR is set to 0x000FFC00.
[*3] Used by REALOS
[*4] ICR23 and ICR47 can be exchanged by setting the REALOS compatibility bit (addr 0x0C03 : IOS[0])
[*5] System reserved
[*6] Memory Protection Unit (MPU) support

6 Package and Pin Assignment

6.1 Package

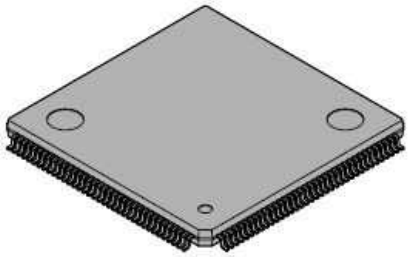
A QFP-144 package will be used for MB91F467BA/466BA/465BA/464BA.
The package code is FPT-144P-M08

FUJITSU SEMICONDUCTOR
DATA SHEET

LOW PROFILE QUAD FLAT PACKAGE
144 PIN PLASTIC

FPT-144P-M08

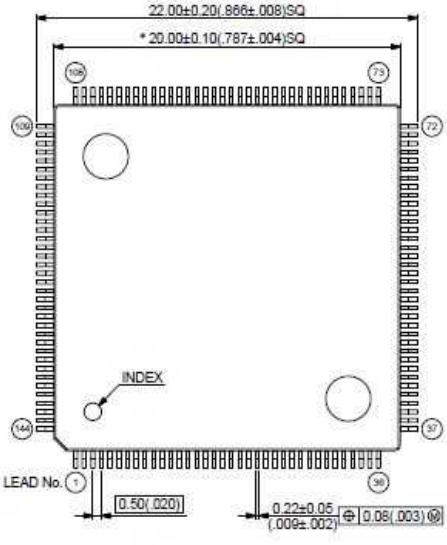
144-pin plastic LQFP



(FPT-144P-M08)

Lead pitch	0.50 mm
Package width × package length	20.0 × 20.0 mm
Lead shape	Gullwing
Sealing method	Plastic mold
Mounting height	1.70 mm MAX
Weight	1.20g
Code (Reference)	P-LFQFP144-20×20-0.50

144-pin plastic LQFP
(FPT-144P-M08)



Note 1) *:Values do not include resin protrusion.
Resin protrusion is +0.25(.010)Max(each side).
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.

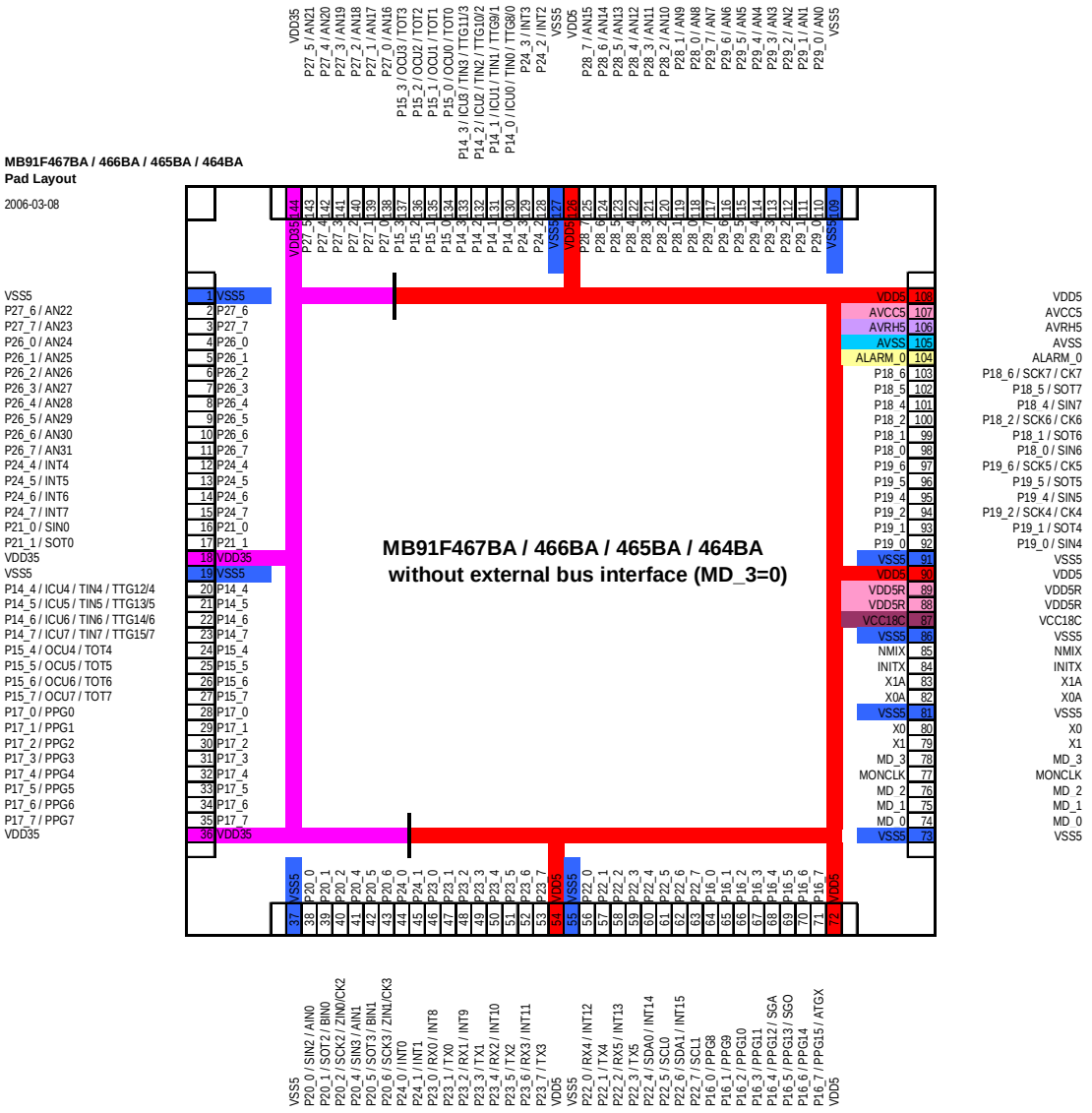
© 2003 FUJITSU LIMITED F144019S-c-4-6

Dimensions in mm (inches).
Note: The values in parentheses are reference values.

The contents of this document are subject to change without notice.
Customers are advised to consult with FUJITSU sales representatives before ordering.
FUJITSU is unable to assume responsibility for infringement of any patent rights or other rights of third parties arising from the use of the information or package dimensions in this document.

6.2 I/O Pins and their functions

6.2.1 MB91F467BA / 466BA / 465BA / 464BA with MD_3 = 0



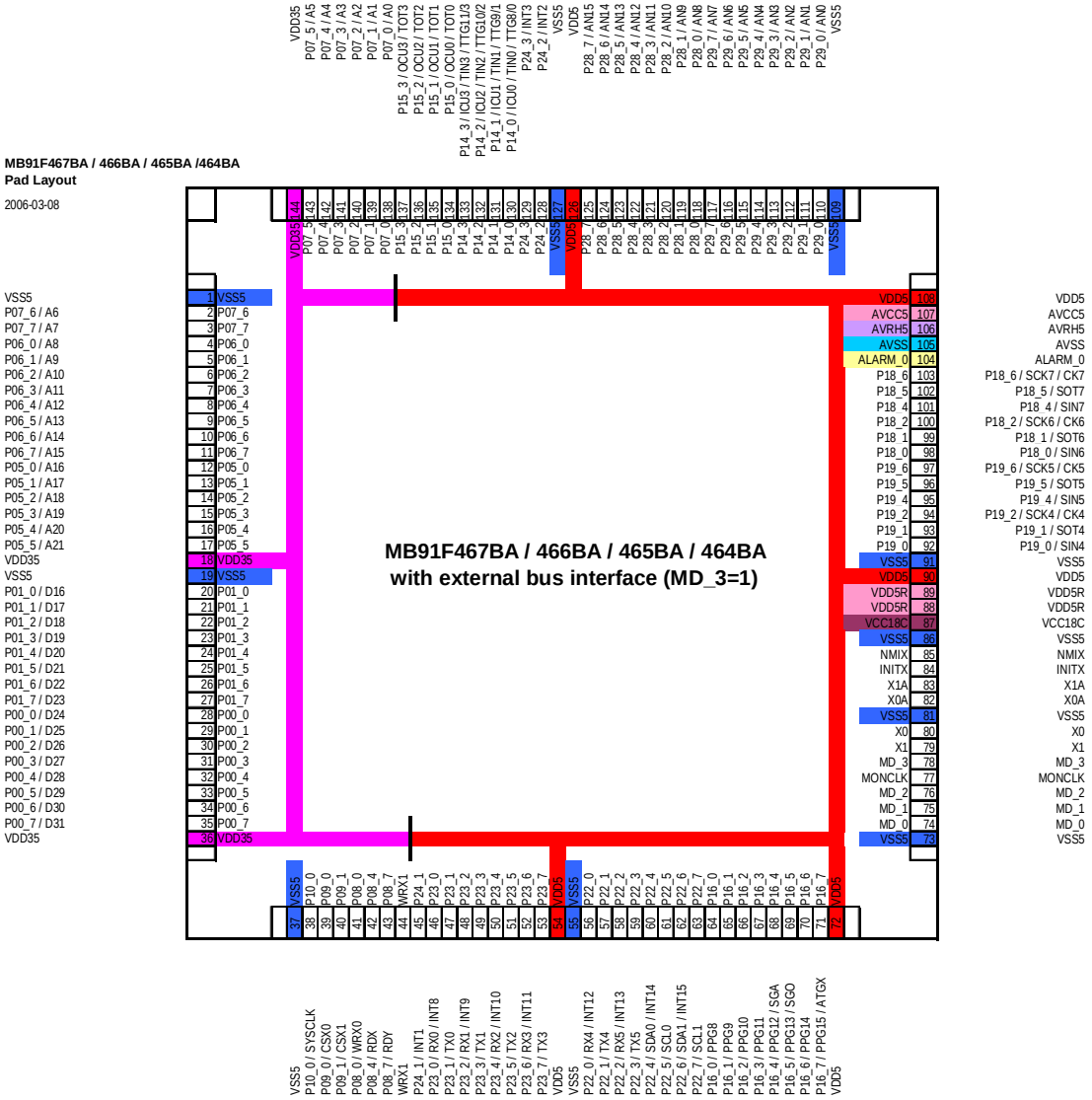
Pin	I/O	PFR=1	EPFR=1	Special	Type	Comments
79	X1	-	-	-	TO00_1	4 MHz quartz oscillator
80	X0	-	-	-	TO00_0	
83	X1A	-	-	-	TO01_1	32 kHz quartz oscillator
82	X0A	-	-	-	TO01_0	
77	MONCLK	-	-	-	TC10_0	Clock monitor output
23	P14_7	ICU7/TIN7	TIN7	TTG15/7	TP04_1	ICU: Input Capture Unit input, TIN: Reload Timer Event input, TTG: Prog. Pulse Generator Event input
22	P14_6	ICU6/TIN6	TIN6	TTG14/6	TP04_1	
21	P14_5	ICU5/TIN5	TIN5	TTG13/5	TP04_1	
20	P14_4	ICU4/TIN4	TIN4	TTG12/4	TP04_1	
133	P14_3	ICU3/TIN3	TIN3	TTG11/3	TP04_0	
132	P14_2	ICU2/TIN2	TIN2	TTG10/2	TP04_0	
131	P14_1	ICU1/TIN1	TIN1	TTG9/1	TP04_0	
130	P14_0	ICU0/TIN0	TIN0	TTG8/0	TP04_0	
27	P15_7	OCU7	TOT7	-	TP04_1	OCU: Output Compare Unit waveform out., TOT: Reload Timer output
26	P15_6	OCU6	TOT6	-	TP04_1	
25	P15_5	OCU5	TOT5	-	TP04_1	
24	P15_4	OCU4	TOT4	-	TP04_1	
137	P15_3	OCU3	TOT3	-	TP04_0	
136	P15_2	OCU2	TOT2	-	TP04_0	
135	P15_1	OCU1	TOT1	-	TP04_0	
134	P15_0	OCU0	TOT0	-	TP04_0	
71	P16_7	PPG15	ATGX	-	TP04_0	PPG: Prog. Pulse Generator waveform out, ATGX: ADC external trigger input, SGO: Sound Generator waveform out, SGA: Sound Generator amplitude out
70	P16_6	PPG14	-	-	TP04_0	
69	P16_5	PPG13	SGO	-	TP04_0	
68	P16_4	PPG12	SGA	-	TP04_0	
67	P16_3	PPG11	-	-	TP04_0	
66	P16_2	PPG10	-	-	TP04_0	
65	P16_1	PPG9	-	-	TP04_0	
64	P16_0	PPG8	-	-	TP04_0	
35	P17_7	PPG7	-	-	TP04_1	PPG: Prog. Pulse Generator waveform out
34	P17_6	PPG6	-	-	TP04_1	
33	P17_5	PPG5	-	-	TP04_1	
32	P17_4	PPG4	-	-	TP04_1	
31	P17_3	PPG3	-	-	TP04_1	
30	P17_2	PPG2	-	-	TP04_1	
29	P17_1	PPG1	-	-	TP04_1	
28	P17_0	PPG0	-	-	TP04_1	
103	P18_6	SCK7	CK7	-	TP04_0	SCK: LIN-USART clock I/O, SIN: LIN-USART serial input, SOT: LIN-USART serial out, CK: Free Run Timer input
102	P18_5	SOT7	-	-	TP04_0	
101	P18_4	SIN7	-	-	TP04_0	

Pin	I/O	PFR=1	EPFR=1	Special	Type	Comments
100	P18_2	SCK6	CK6	-	TP04_0	
99	P18_1	SOT6	-	-	TP04_0	
98	P18_0	SIN6	-	-	TP04_0	
97	P19_6	SCK5	CK5	-	TP04_0	SCK: LIN-USART clock I/O, SIN: LIN-USART serial input, SOT: LIN-USART serial out, CK: Free Run Timer input
96	P19_5	SOT5	-	-	TP04_0	
95	P19_4	SIN5	-	-	TP04_0	
94	P19_2	SCK4	CK4	-	TP04_0	
93	P19_1	SOT4	-	-	TP04_0	
92	P19_0	SIN4	-	-	TP04_0	
43	P20_6	SCK3	ZIN1/CK3	-	TP04_0	SCK: LIN-USART clock I/O, SIN: LIN-USART serial input, SOT: LIN-USART serial out, CK: Free Run Timer input, AIN: Up-Down Counter up-count input, BIN: Up-Down Counter down-count input, ZIN: Up-Down Counter reset input
42	P20_5	SOT3	BIN1	-	TP04_0	
41	P20_4	SIN3	AIN1	-	TP04_0	
40	P20_2	SCK2	ZIN0/CK2	-	TP04_0	
39	P20_1	SOT2	BIN0	-	TP04_0	
38	P20_0	SIN2	AIN0	-	TP04_0	
17	P21_1	SOT0	-	-	TP04_0	SIN: LIN-USART serial input, SOT: LIN-USART serial out
16	P21_0	SIN0	-	-	TP04_0	
63	P22_7	SCL1	-	-	TP02_0	SCL: I2C serial clock I/O, SDA: I2C serial data I/O, INT: External Interrupt input TX: CAN transmission I/O, RX: CAN reception input, INT: External Interrupt input
62	P22_6	SDA1	-	INT15	TP02_0	
61	P22_5	SCL0	-	-	TP02_0	
60	P22_4	SDA0	-	INT14	TP02_0	
59	P22_3	TX5	-	-	TP04_0	
58	P22_2	RX5	-	INT13	TP04_0	
57	P22_1	TX4	-	-	TP04_0	
56	P22_0	RX4	-	INT12	TP04_0	
53	P23_7	TX3	-	-	TP04_0	TX: CAN transmission I/O, RX: CAN reception input, INT: External Interrupt input
52	P23_6	RX3	-	INT11	TP04_0	
51	P23_5	TX2	-	-	TP04_0	
50	P23_4	RX2	-	INT10	TP04_0	
49	P23_3	TX1	-	-	TP04_0	
48	P23_2	RX1	-	INT9	TP04_0	
47	P23_1	TX0	-	-	TP04_0	
46	P23_0	RX0	-	INT8	TP04_0	
15	P24_7	INT7	-	-	TP04_0	INT: External Interrupt input
14	P24_6	INT6	-	-	TP04_0	
13	P24_5	INT5	-	-	TP04_0	
12	P24_4	INT4	-	-	TP04_0	
129	P24_3	INT3	-	-	TP04_0	
128	P24_2	INT2	-	-	TP04_0	
45	P24_1	INT1	-	-	TP04_0	
44	P24_0	INT0	-	-	TP04_0	

Pin	I/O	PFR=1	EPFR=1	Special	Type	Comments
11	P26_7	-	AN31	-	TP03_0	AN: ADC Analog input
10	P26_6	-	AN30	-	TP03_0	
9	P26_5	-	AN29	-	TP03_0	
8	P26_4	-	AN28	-	TP03_0	
7	P26_3	-	AN27	-	TP03_0	
6	P26_2	-	AN26	-	TP03_0	
5	P26_1	-	AN25	-	TP03_0	
4	P26_0	-	AN24	-	TP03_0	
3	P27_7	-	AN23	-	TP03_0	AN: ADC Analog input
2	P27_6	-	AN22	-	TP03_0	
143	P27_5	-	AN21	-	TP03_0	
142	P27_4	-	AN20	-	TP03_0	
141	P27_3	-	AN19	-	TP03_0	
140	P27_2	-	AN18	-	TP03_0	
139	P27_1	-	AN17	-	TP03_0	
138	P27_0	-	AN16	-	TP03_0	
104	ALARM_0	-	-	-	TA02_0	ALARM Comparator input
125	P28_7	AN15	-	-	TP03_0	AN: ADC Analog input
124	P28_6	AN14	-	-	TP03_0	
123	P28_5	AN13	-	-	TP03_0	
122	P28_4	AN12	-	-	TP03_0	
121	P28_3	AN11	-	-	TP03_0	
120	P28_2	AN10	-	-	TP03_0	
119	P28_1	AN9	-	-	TP03_0	
118	P28_0	AN8	-	-	TP03_0	
117	P29_7	AN7	-	-	TP03_0	AN: ADC Analog input
116	P29_6	AN6	-	-	TP03_0	
115	P29_5	AN5	-	-	TP03_0	
114	P29_4	AN4	-	-	TP03_0	
113	P29_3	AN3	-	-	TP03_0	
112	P29_2	AN2	-	-	TP03_0	
111	P29_1	AN1	-	-	TP03_0	
110	P29_0	AN0	-	-	TP03_0	
84	INITX	-	-	-	TC02_0	Reset pin (low active)
85	NMIX	-	-	-	TC02_0	NMI pin (low active)
78	MD_3	-	-	-	TC02_0	Mode pin for external bus interface option
76	MD_2	-	-	-	TC01_0	Mode pins
75	MD_1	-	-	-	TC01_0	
74	MD_0	-	-	-	TC01_0	
54 72	VDD5	-	-	-	TS02_0	Power Supply for I/O ring 5 V

Pin	I/O	PFR=1	EPFR=1	Special	Type	Comments
90 108 126						
18 36 144	VDD35	-	-	-	TS02_0	Power Supply for external bus part of IO ring
88 89	VDD5R	-	-	-	TA00_0	Power supply for Voltage Regulator/Core 5V
1 19 37 55 73 81 86 91 109 127	VSS5	-	-	-	TS00_0	Ground Supply
107	AVCC5	-	-	-	TA00_0	Analog Power supply 5 V
106	AVRH5	-	-	-	TA01_0	Analog High Reference 5 V
105	AVSS	-	-	-	TA03_0	Analog Ground supply + Low Reference
87	VCC18C	-	-	-	TA10_0	Voltage Regulator Capacitance pin

6.2.2 MB91F467BA / 466BA / 465BA / 464BA with MD_3 = 1



Pin	I/O	PFR=1	EPFR=1	Special	Type	Comments
79	X1	-	-	-	TO00_1	4 MHz quartz oscillator
80	X0	-	-	-	TO00_0	
83	X1A	-	-	-	TO01_1	32 kHz quartz oscillator
82	X0A	-	-	-	TO01_0	
77	MONCLK	-	-	-	TC10_0	Clock monitor output
133	P14_3	ICU3/TIN3	TIN3	TTG11/3	TP04_0	ICU: Input Capture Unit input, TIN: Reload Timer Event input, TTG: Prog. Pulse Generator Event input
132	P14_2	ICU2/TIN2	TIN2	TTG10/2	TP04_0	
131	P14_1	ICU1/TIN1	TIN1	TTG9/1	TP04_0	
130	P14_0	ICU0/TIN0	TIN0	TTG8/0	TP04_0	
137	P15_3	OCU3	TOT3	-	TP04_0	OCU: Output Compare Unit waveform out., TOT: Reload Timer output
136	P15_2	OCU2	TOT2	-	TP04_0	
135	P15_1	OCU1	TOT1	-	TP04_0	
134	P15_0	OCU0	TOT0	-	TP04_0	
71	P16_7	PPG15	ATGX	-	TP04_0	PPG: Prog. Pulse Generator waveform out, ATGX: ADC external trigger input, SGO: Sound Generator waveform out, SGA: Sound Generator amplitude out
70	P16_6	PPG14	-	-	TP04_0	
69	P16_5	PPG13	SGO	-	TP04_0	
68	P16_4	PPG12	SGA	-	TP04_0	
67	P16_3	PPG11	-	-	TP04_0	
66	P16_2	PPG10	-	-	TP04_0	
65	P16_1	PPG9	-	-	TP04_0	
64	P16_0	PPG8	-	-	TP04_0	
103	P18_6	SCK7	CK7	-	TP04_0	SCK: LIN-USART clock I/O, SIN: LIN-USART serial input, SOT: LIN-USART serial out, CK: Free Run Timer input
102	P18_5	SOT7	-	-	TP04_0	
101	P18_4	SIN7	-	-	TP04_0	
100	P18_2	SCK6	CK6	-	TP04_0	
99	P18_1	SOT6	-	-	TP04_0	
98	P18_0	SIN6	-	-	TP04_0	
97	P19_6	SCK5	CK5	-	TP04_0	SCK: LIN-USART clock I/O, SIN: LIN-USART serial input, SOT: LIN-USART serial out, CK: Free Run Timer input
96	P19_5	SOT5	-	-	TP04_0	
95	P19_4	SIN5	-	-	TP04_0	
94	P19_2	SCK4	CK4	-	TP04_0	
93	P19_1	SOT4	-	-	TP04_0	
92	P19_0	SIN4	-	-	TP04_0	
63	P22_7	SCL1	-	-	TP02_0	SCL: I2C serial clock I/O, SDA: I2C serial data I/O, INT: External Interrupt input TX: CAN transmission I/O, RX: CAN reception input, INT: External Interrupt input
62	P22_6	SDA1	-	INT15	TP02_0	
61	P22_5	SCL0	-	-	TP02_0	
60	P22_4	SDA0	-	INT14	TP02_0	
59	P22_3	TX5	-	-	TP04_0	
58	P22_2	RX5	-	INT13	TP04_0	
57	P22_1	TX4	-	-	TP04_0	

Pin	I/O	PFR=1	EPFR=1	Special	Type	Comments
56	P22_0	RX4	-	INT12	TP04_0	
53	P23_7	TX3	-	-	TP04_0	TX: CAN transmission I/O, RX: CAN reception input, INT: External Interrupt input
52	P23_6	RX3	-	INT11	TP04_0	
51	P23_5	TX2	-	-	TP04_0	
50	P23_4	RX2	-	INT10	TP04_0	
49	P23_3	TX1	-	-	TP04_0	
48	P23_2	RX1	-	INT9	TP04_0	
47	P23_1	TX0	-	-	TP04_0	
46	P23_0	RX0	-	INT8	TP04_0	
129	P24_3	INT3	-	-	TP04_0	INT: External Interrupt input
128	P24_2	INT2	-	-	TP04_0	
45	P24_1	INT1	-	-	TP04_0	
104	ALARM_0	-	-	-	TA02_0	ALARM Comparator input
125	P28_7	AN15	-	-	TP03_0	AN: ADC Analog input
124	P28_6	AN14	-	-	TP03_0	
123	P28_5	AN13	-	-	TP03_0	
122	P28_4	AN12	-	-	TP03_0	
121	P28_3	AN11	-	-	TP03_0	
120	P28_2	AN10	-	-	TP03_0	
119	P28_1	AN9	-	-	TP03_0	
118	P28_0	AN8	-	-	TP03_0	
117	P29_7	AN7	-	-	TP03_0	AN: ADC Analog input
116	P29_6	AN6	-	-	TP03_0	
115	P29_5	AN5	-	-	TP03_0	
114	P29_4	AN4	-	-	TP03_0	
113	P29_3	AN3	-	-	TP03_0	
112	P29_2	AN2	-	-	TP03_0	
111	P29_1	AN1	-	-	TP03_0	
110	P29_0	AN0	-	-	TP03_0	
35	P00_7	D31	-	-	TP04_1	External Bus Data Lines
34	P00_6	D30	-	-	TP04_1	
33	P00_5	D29	-	-	TP04_1	
32	P00_4	D28	-	-	TP04_1	
31	P00_3	D27	-	-	TP04_1	
30	P00_2	D26	-	-	TP04_1	
29	P00_1	D25	-	-	TP04_1	
28	P00_0	D24	-	-	TP04_1	
27	P01_7	D23	-	-	TP04_1	External Bus Data Lines
26	P01_6	D22	-	-	TP04_1	
25	P01_5	D21	-	-	TP04_1	
24	P01_4	D20	-	-	TP04_1	

Pin	I/O	PFR=1	EPFR=1	Special	Type	Comments
23	P01_3	D19	-	-	TP04_1	
22	P01_2	D18	-	-	TP04_1	
21	P01_1	D17	-	-	TP04_1	
20	P01_0	D16	-	-	TP04_1	
138	P07_0	A0	-	-	TP03_0	External Bus Address Lines
139	P07_1	A1	-	-	TP03_0	
140	P07_2	A2	-	-	TP03_0	
141	P07_3	A3	-	-	TP03_0	
142	P07_4	A4	-	-	TP03_0	
143	P07_5	A5	-	-	TP03_0	
2	P07_6	A6	-	-	TP03_0	
3	P07_7	A7	-	-	TP03_0	
4	P06_0	A8	-	-	TP03_0	External Bus Address Lines
5	P06_1	A9	-	-	TP03_0	
6	P06_2	A10	-	-	TP03_0	
7	P06_3	A11	-	-	TA03_0	
8	P06_4	A12	-	-	TP03_0	
9	P06_5	A13	-	-	TP03_0	
10	P06_6	A14	-	-	TP03_0	
11	P06_7	A15	-	-	TP03_0	
12	P05_0	A16	-	-	TP04_0	External Bus Address Lines
13	P05_1	A17	-	-	TP04_0	
14	P05_2	A18	-	-	TP04_0	
15	P05_3	A19	-	-	TP04_0	
16	P05_4	A20	-	-	TP04_0	
17	P05_5	A21	-	-	TP04_0	
39	P09_0	CSX0	-	-	TP04_0	External Bus Control Signals
40	P09_1	CSX1	-	-	TP04_0	
41	P08_0	WRX0	-	-	TP04_0	
42	P08_4	RDX	-	-	TP04_0	
43	P08_7	RDY	-	-	TP04_0	
44	WRX1 *1	- *1	-	-	TP04_0	
38	P10_0	SYSCLK	-	-	TP04_0	
84	INITX	-	-	-	TC02_0	Reset pin (low active)
85	NMIX	-	-	-	TC02_0	NMI pin (low active)
78	MD_3	-	-	-	TC02_0	Mode pin for external bus interface option
76	MD_2	-	-	-	TC01_0	Mode pins
75	MD_1	-	-	-	TC01_0	
74	MD_0	-	-	-	TC01_0	
54 72	VDD5	-	-	-	TS02_0	Power Supply for I/O ring 5 V

Pin	I/O	PFR=1	EPFR=1	Special	Type	Comments
90 108 126						
18 36 144	VDD35	-	-	-	TS02_0	Power Supply for external bus part of IO ring
88 89	VDD5R	-	-	-	TA00_0	Power supply for Voltage Regulator/Core 5V
1 19 37 55 73 81 86 91 109 127	VSS5	-	-	-	TS00_0	Ground Supply
107	AVCC5	-	-	-	TA00_0	Analog Power supply 5 V
106	AVRH5	-	-	-	TA01_0	Analog High Reference 5 V
105	AVSS	-	-	-	TA03_0	Analog Ground supply + Low Reference
87	VCC18C	-	-	-	TA10_0	Voltage Regulator Capacitance pin

*1 : There is the following limitation.

********** Limitation **********

In MB91F467BA/466BA/465BA/464BA, you can not use Pin44 as general purpose port

in a state of “MD_3 = 1”. It means that Pin44 is able to use only as “WRX1”.

(For a description of I/O Ports please refer to Hardware Manual chapter 55.)

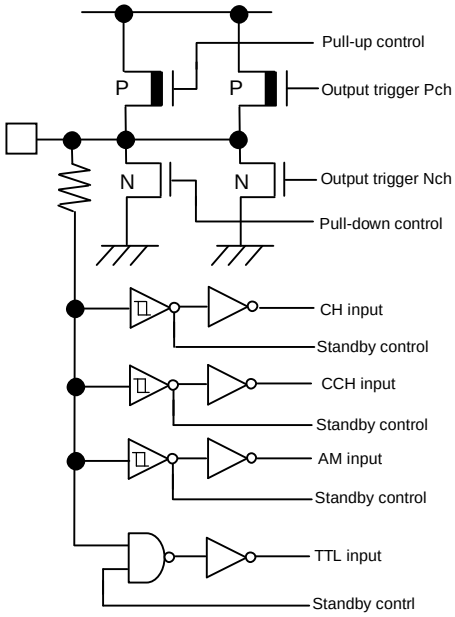
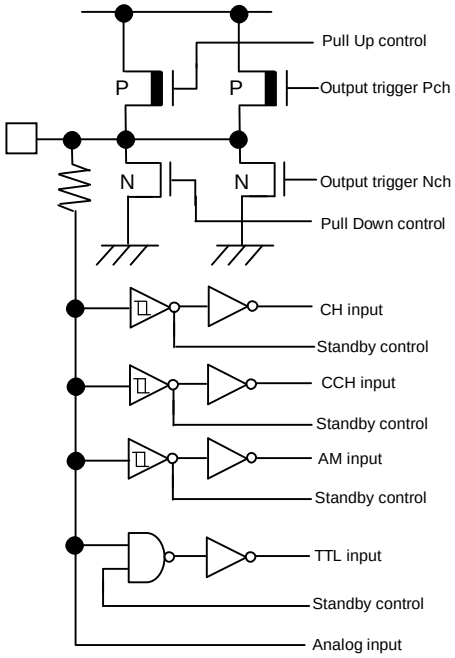
****

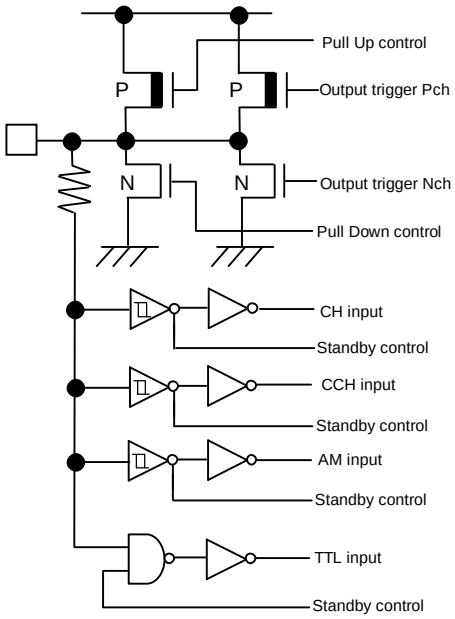
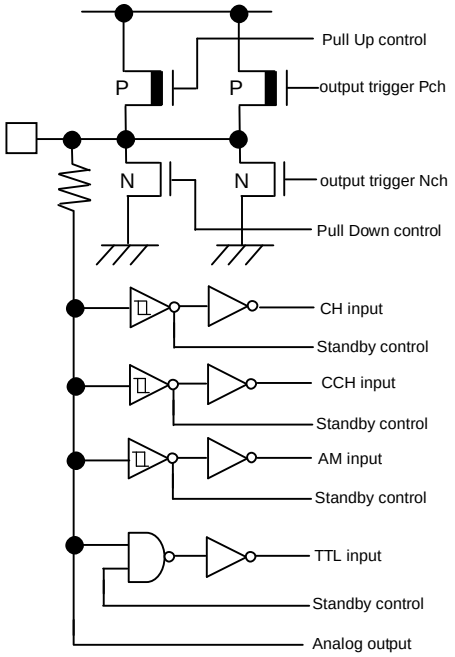
6.3 I/O Pin Types

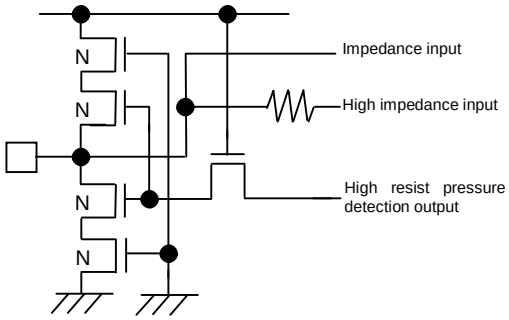
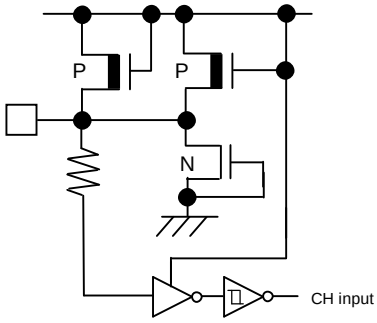
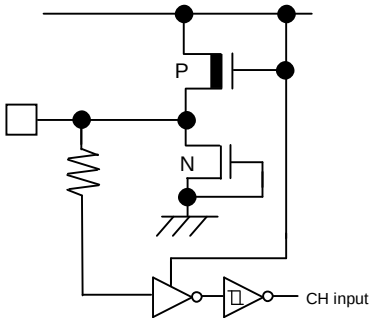
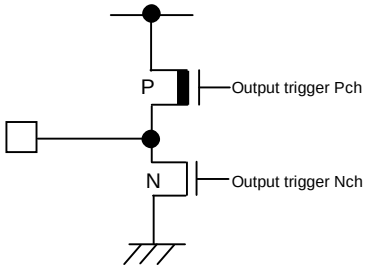
Pin Type	Pull Up/ Down	Input Type	STOP control	Output Driver	Comment
TP02_0	U/D control	CH / A / TTL / CH2	Stop	3 mA	I2C Pin (open drain if PFR=1)
TP03_0	U/D control	CH / A / TTL / CH2	Stop	2/5 mA	General Purpose I/O with 1 analog input line
TP04_0	U/D control	CH / A / TTL / CH2	Stop	2/5 mA	General Purpose I/O
TP04_1	U/D control	CH / A / TTL / CH2	Stop	2/5 mA	General Purpose I/O with 1 analog output line
TC01_0	-	C2	no	-	Mode Pin (MD_2, MD_1, MD_0)
TC02_0	Up	C2	no	-	Input pin (INITX, NMIX)
TC02_1		C2	no	-	Input pin (MD_3)
TC10_0	-	-	no	5 mA	Threestate Output port 5mA for MONCLK
TO00_0 TO00_1	-	-	-	-	4 MHz Oscillator Pin
TO01_0 TO01_1	-	-	-	-	32 KHz Oscillator Pin
TA00_0	-	-	-	-	Analog power supply pin
TA01_0	-	-	-	-	Analog I/O pin
TA02_0	-	-	-	-	Analog I/O pin
TA03_0	-	-	-	-	Analog Ground pin

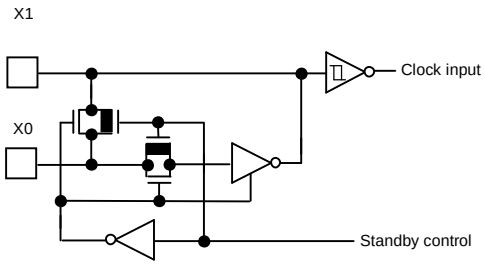
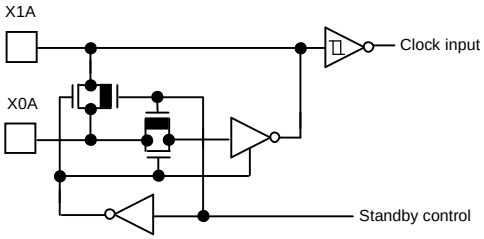
Notes:

- The pull-up / pull-down resistors are typical 50 kOhm.
  The controlled pull-up/down's can be enabled by register setting.
- Input Types: CH CMOS Schmitt trigger
  CH2 CMOS Schmitt trigger 2
  A CMOS Automotive Schmitt trigger
  TTL TTL
  (for input high/low voltages, please see section Operating Conditions)
- Stop control: Switch to HiZ in STOP mode by register setting, and disable input lines in STOP if the port is not configuerd to be external interrupt input.
- Default output driver strength is 3 mA (I2C pins) and 5 mA (all other pins).

Pin Type	Citcuit	Comment
TP02_0		• I^2C combined use General Purpose I/O (I^2C Pin : open drain if PFR=1) • Pull-up Resistor (50 kΩ) with control • Pull-down Resistor (50 kΩ) with control • I_{OH} = 3mA, I_{OL} = 3mA • CMOS Schmitt trigger input ($0.8V_{CC}/0.2V_{CC}$) with standby control (If standby assert, CH input keeps previous value.) • CMOS Schmitt trigger input ($0.7V_{CC}/0.3V_{CC}$) with standby control (If standby assert, CCH input keeps previous value.) • CMOS Automotive Schmitt trigger input ($0.8V_{CC}/0.5V_{CC}$) with standby control (If standby assert, AM input keeps previous value.) • TTL input (2.0V/0.8V) with standby control (If standby assert, TTL input becomes 'L')
TP03_0		• AD combined use General Purpose I/O • Pull-up Resistor (50 kΩ) with control • Pull-down Resistor (50 kΩ) with control • I_{OH} = 2/5mA, I_{OL} = 2/5mA • CMOS Schmitt trigger input ($0.8V_{CC}/0.2V_{CC}$) with standby control (If standby assert, CH input keeps previous value.) • CMOS Schmitt trigger input ($0.7V_{CC}/0.3V_{CC}$) with standby control (If standby assert, CCH input keeps previous value.) • CMOS Automotive Schmitt trigger input ($0.8V_{CC}/0.5V_{CC}$) with standby control (If standby assert, AM input keeps previous value.) • TTL input (2.0V/0.8V) with standby control (If standby assert, TTL input becomes 'L') • Analog input for AD converter

Pin Type	Citcuit	Comment
TP04_0		• General Purpose I/O • Pull-up Resistor (50 kΩ) with control • Pull-down Resistor (50 kΩ) with control • I_{OH} = 2/5mA, I_{OL} = 2/5mA • CMOS Schmitt trigger input ($0.8V_{CC}/0.2V_{CC}$) with standby control (If standby assert, CH input keeps previous value.) • CMOS Schmitt trigger input ($0.7V_{CC}/0.3V_{CC}$) with standby control (If standby assert, CCH input keeps previous value.) • CMOS Automotive Schmitt trigger input ($0.8V_{CC}/0.5V_{CC}$) with standby control (If standby assert, AM input keeps previous value.) • TTL input (2.0V/0.8V) with standby control (If standby assert, TTL input becomes 'L')
TP04_1		• General Purpose I/O with Analog output • Pull-up Resistor (50 kΩ) with control • Pull-down Resistor (50 kΩ) with control • I_{OH} = 2/5mA, I_{OL} = 2/5mA • CMOS Schmitt trigger input ($0.8V_{CC}/0.2V_{CC}$) with standby control (If standby assert, CH input keeps previous value.) • CMOS Schmitt trigger input ($0.7V_{CC}/0.3V_{CC}$) with standby control (If standby assert, CCH input keeps previous value.) • CMOS Automotive Schmitt trigger input ($0.8V_{CC}/0.5V_{CC}$) with standby control (If standby assert, AM input keeps previous value.) • TTL input (2.0V/0.8V) with standby control (If standby assert, TTL input becomes 'L')

Pin Type	Citcuit	Comment
TC01_0		• CMOS Input • High resist pressure Input
TC02_0		• CMOS Schmitt-Trigger Input • Pull up Resistor : 50kΩ
TC02_1		• CMOS Schmitt-Trigger Input
TC10_0		• Threestate Output • I_{OH} = 5mA, I_{OL} = 5mA

Pin Type	Citcuit	Comment
TO00_0 TO00_1		• 4 MHz Oscillator Pin (with standby control)
TO01_0 TO01_1		• 32 KHz Oscillator Pin (with standby control)

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Parameter	Symbol	min.	max.	Unit	Condition
Digital supply voltage	VDD-VSS	-0.3	6.0	V	
Stepper motor control supply voltage	HVDD-HVSS	-0.3	6.0	V	
Storage temperature	T_{ST}	-55	125	°C	
Power consumption	P_{TOT}		1000	mW	T_A = 25°C
Digital input voltage	V_{IDIG}	-0.3 *	5.8	V	VSS=0V, VDD=5V
Analogue input voltage	V_{IA}	-0.3	5.8	V	AVSS=0V, AVCC=5V
Analogue supply voltage	AVCC - AVSS	-0.3	5.8	V	AVSS=0V
Analogue reference voltage	AVRH - AVSS	-0.3	5.8	V	AVSS=0V
Static DC current into digital I/O	$I_{I/ODC}$	-2	2	mA	$\Sigma I_{I/ODC} < I_{SRUN}$

***** Making full use of the allowed static DC current into digital I/Os will lead to lower values here.

7.2 Operating Conditions

Parameter	Symbol	min.	typ.	max.	Unit	Condition
Operating temperature	T_{OP}	-40		105	°C	
Supply voltage						Internal voltage reg.
- Digital supply	VDD5-VSS	3.0		5.5	V	VDD_{CORE}=1.8V
- External bus supply	VDD35-VSS	3.0		5.5	V	
- Analog supply	AVCC-AVSS	3.0		5.5	V	AVSS=0V
Current consumption						T_A = 25°C,
-run mode	I_{srun}		140		mA	VSS=0V,VDD=5V
-RTC mode	I_{sRTC}		100 40		µA µA	f =4MHz f <= 100kHz
-stop mode	I_{sstop}		30		µA	
Alarm comparator						
-Threshold voltages						
- overvoltage	V_{TAH}	$^4/_5$ AVCC-5%	$^4/_5$AVCC	$^4/_5$ AVCC+5%	V	(external 4:1 divider)
- undervoltage	V_{TAL}	$^2/_5$ AVCC-5%	$^2/_5$AVCC	$^2/_5$ AVCC+5%	V	
- Switching hysteresis	V_{TAHYS}	100		200	mV	at V_{TAH}, V_{TAL}
- Alarm sense time	t_{AS}			0.1/100[3)]	µs	selectable by register
- Input resistance	R_{in}	5			MΩ	
Digital Inputs [1)]						
CMOS Schmitt-Trigger						
- High voltage range	V_{IH}	0.7*VDD		VDD	V	
- Low voltage range	V_{IL}	VSS		0.3*VDD	V	
CMOS Automotive Schmitt-Trigger						
- High voltage range	V_{IH}	0.8*VDD		VDD	V	
- Low voltage range	V_{IL}	VSS		0.5*VDD	V	
- hysteresis voltage		0.2		0.5	V	
- Input capacitance	C_{IN}			tbd	pF	
- Input leakage current	I_{IL}	-1		1	µA	
- Pull up resistor	R_{up}		50		kΩ	
- Pull down resistor	R_{down}		50		kΩ	T_{op}=25 deg. C
Digital outputs						
- Output "H" voltage	V_{OH}	VDD-0.5		VDD	V	I_{load} = 2/ 5mA
- Output "L" voltage	V_{OL}	VSS		VSS+0.4	V	I_{load} = - 2/-5mA

Parameter	Symbol	min.	typ.	max.	Unit	Condition
ADC inputs [2)]						
- Reference voltage input	AVRH AVRL	AVCC*0.75 AVSS		AVCC AVCC*0.25	V V	
- Input voltage range	V_{imax} V_{imin}	 AVRL		AVRH	V V	
- Input resistance	R_I			10	kΩ	
- Input capacitance	C_I			17	pF	
- Impedance of external output driving the ADC input				4.0	kΩ	@ sampling time of 1.6 µs and AVCC >= 4.5V
- Input leakage current	I_{IL}	-1		1	µA	T_{op}=25 deg. C
Sound generator						
- Output voltage	$V_{outHIGH}$ V_{outLOW}	VDD-0.5 VSS		VDD VSS+0.5	V V	
- Output current	I_{out}	5			mA	
PPG						
- Output voltage	$V_{outHIGH}$ V_{outLOW}	VDD-0.5 VSS		VDD VSS+0.5	V V	
- Output current	I_{out}	5			mA	
I^2C Bus Interface						Open Drain Output
- Output voltage	$V_{outHIGH}$ V_{outLOW}	 VSS		VDD VSS+0.5	V V	I_{outLOW}= 3mA
- Output current	I_{out}	3			mA	
Lock-up time PLL1 (4MHz->16…96MHz)			0.1	0.2	ms	

[1)] valid for bidirectional tristate I/O PAD cell

[2)] The protection diodes at the analog inputs are connected to the digital supply voltage

[3)] The longer alarm sense time can be selected for power safe modes in order to reduce the current consumption

7.3 Converter Characteristics

- A/D Converter

Parameter	Symbol	Rating			Unit	Remark
		Minimum	Typical	Maximum		
Resolution				10	Bit	
Conversion error				+/- 3.0	LSB	Overall error
Non-linearity				+/-2.5	LSB	
Differential Non-linearity				+/-1.9	LSB	
Zero Reading voltage	V_{0T}	AVRL -1.5	AVRL+0.5	AVRL+2.5	LSB	
Full scale reading voltage	V_{FST}	AVRH-3.5	AVRH-1.5	AVRH+0.5	LSB	
Input current	IA @ AVCC		2.4	4.7	mA	
Reference voltage current	IR		0.65	1.0	mA	